PROCEEDINGS OF SCIENCE

System Testing of the CMS Endcap MIP Timing Layer

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The high luminosity phase of the LHC (HL-LHC) opens up new windows for exciting discoveries but also brings about new challenges due to the high pileup environment of approximately 200 simultaneous interactions per collision. Precise measurements of track and vertex timing can efficiently mitigate these pileup effects. Therefore, the CMS detector will be upgraded with a MIP timing detector (MTD) capable of providing ultra-fast timing information of trajectories of charged particles. With a time resolution of below 50 ps per hit the MTD will be a key ingredient to discover new physics at the HL-LHC. The endcap region of the MTD ($1.6 < |\eta| < 3.0$) has to endure high fluences, motivating the use of thin radiation tolerant silicon sensors with fast charge collection. Tests and developments of these low gain avalanche diodes (LGADs) by CMS together with manufacturers have resulted in a robust design of 16x16 pixel sensors. A custom readout chip for ETL sensors (ETROC) containing clock trees, preamplifier, discriminator, and TDC is being developed in parallel. Several testing campaigns were carried out in the last year, from test beams to characterize the performance of the ETROC2 prototypes together with bump bonded LGAD sensors, to initial tests of the full system, including front end electronics and back end prototypes.

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1. Introduction

In 2029, the High-luminosity LHC (HL-LHC) will have to face a more challenging pile up environment, with the number of interactions per bunch crossing increasing from approximately 70 to 200. Under these conditions, the population of tracks and energy deposits will increase, degrading the efficiency of reconstruction and identification of the primary hard scatter interaction. To address this problem, the Compact Muon Solenoid (CMS) detector will be updated to use timing measurements to resolve vertices overlapping in space.

In order to maintain the Run 2 physics performance, a precision of 30-50 ps per track is required. The future phase-2 CMS detector will include a new dedicated detector for precision timing of minimum ionizing particles (MIP), known as the MIP timing detector (MTD) [1], which aims to achieve this level of accuracy. The MTD is a thin detector placed between tracker and ECAL, divided into the Barrel Timing Layer (BTL) and two Endcap Timing Layers (ETL). These proceedings focus on the ETL detector and summarize recent testing campaigns that were conducted in 2024 to characterize the performance of the full system (front-end electronics and back-end prototypes).

2. The Endcap MIP Timing Layer

The ETL detector will be mounted outside the inner tracker, on the nose of the Endcap Calorimeter (CE), in a region with high radiation levels, up to $1 \cdot 10^{15}$ n_{eq}/cm^2. Two disks will be installed at each side, covering $1.6 < |\eta| < 3.0$, providing up to two hits per track. The radius of each disk will provide coverage from $315 < r < 1200$ mm, placed at longitudinal positions of $z = \pm 3$ m. The full assembly encompass a total of 8000 modules, with 4 assemblies per module, providing 8 million channels to detect the MIPs.

2.1 Low Gain Avalanche Diodes (LGADs)

To cope with the high radiation levels, the ETL modules will use Ultra-Fast Silicon Detectors (UFSD) based on Low Gain Avalanche Diodes (LGADs) technology [2, 3]. LGADs are relatively thin silicon sensors with low internal gain and low noise, meeting the specifications required to operate with sufficient radiation resistance, maintaining the performance until the end of operations. Each sensor will be a 16x16 array with 1.3x1.3 mm^2 pads. One ETL module PCB unit will contain four sensors.

LGADs are expected to deliver a single hit time resolution of 30 ps for charge depositions in the range of 15-35 fC. The resolution specifications will be maintained over their lifetime, reaching an end-of-time resolution of 40 ps compensating the gain lost with an increase in the supplied bias voltage (BV).

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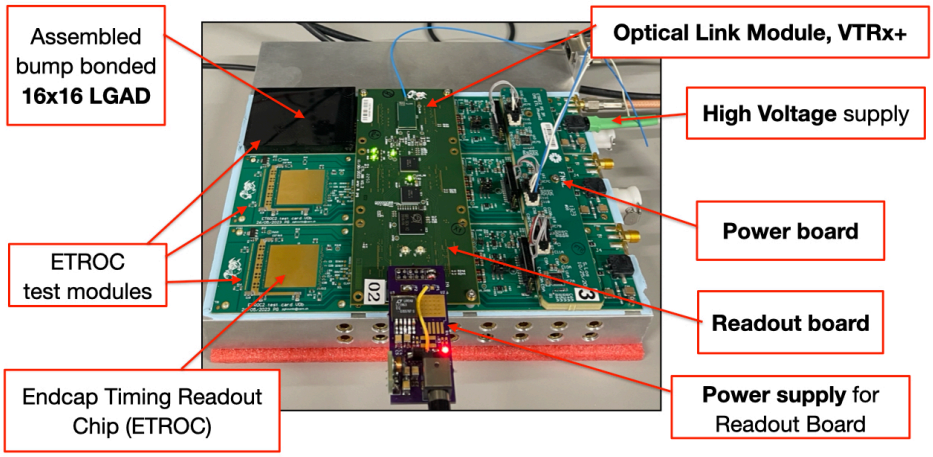

Figure 1: Photo of the ETL module testing setup showing three ETL custom test boards connected to a readout board. The readout board is connected to an optical link module VTRx+ coupled to a fiber. The upper test boards has an assembled 16x16 LGAD bump bonded to an ETROC. Low voltage is supplied to the modules either through the readout board or by an external power board, while high bias voltage is provided externally.

2.2 Readout and Front-End Electronics

The LGAD sensors are readout by a custom designed Endcap Timing Readout Chip (ETROC), containing clock trees, preamplifier, discriminator, and TDC. It is composed of 16x16 pixels, bump-bonded to the sensors pads. The ETROC is then wire-bonded to the module PCB.

In order to read and control the ETROCS and provide fast control, a readout board, based on a GBT chip-set and Optical Link Module VTRx+ [4], is being deployed. The current version of the readout board (RBv2) employed for system testing being presented in these proceedings utilizes SCA-GBT chips for channel monitoring, but future versions will include a MUX64 chip allowing more channels to read.

Additionally, a custom test board taking one single ETROC was designed with the purpose of studying the ETROC + LGAD readout. This test board allows for both external bias voltage (BV) supply, generation of external reference voltage to be used by the ETROC, connections with an external power board or the possibility of wire-bonding 4x4 reduced size LGADs among other functionalities that are used at the current stage for testing purposes. The results presented in these proceedings were obtained with these test cards. The system testing stand, containing all these elements, is presented in Figure 1.

3. System Testing

The modules have been tested in several test beam campaigns performed at both DESY and SPS facilities. Figures 2a and 2b show a photo of the testing setup and an scheme of the elements involved in the data acquisition (DAQ) in the SPS test beam campaign with a pion beam at 120 GeV.

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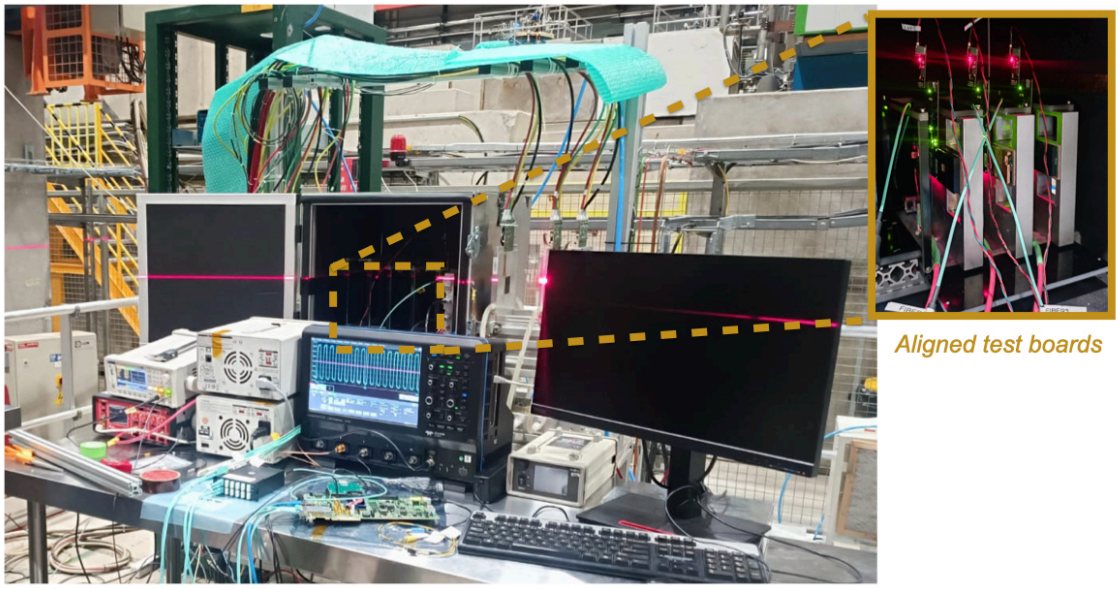
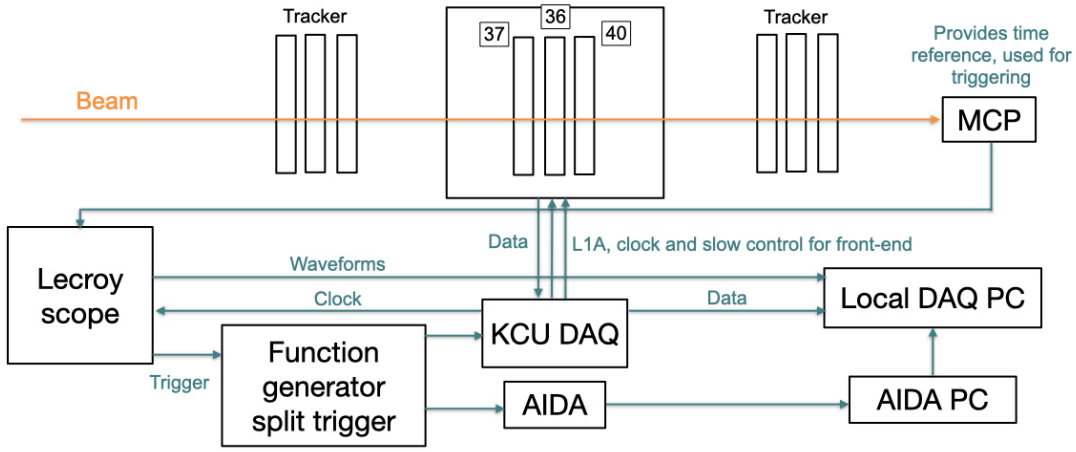


(a) Photo of the elements of the SPS test beam setup.



(b) Scheme of the DAQ employed in the SPS test beam.

Figure 2: Test beam setup mounted in SPS (CERN, May 2024).

The modules are placed inside a cold box where they are aligned with the incoming beam. The three layers of the AIDA tracker [5] are left at each side of the cold box, allowing for the reconstruction the incident pion tracks. The DAQ is controlled using a FPGA KCU105, which sends L1A (trigger) signals to collect data from the modules, generates the 40 MHz clock, and provides slow control for the front-end electronics. A Multi Channel Plate (MCP) photomultiplier, placed after the modules and aligned with the beam, is used for triggering. Whenever the MCP detects a signal, it sends it to an oscilloscope, which sends a trigger to the KCU and to the AIDA tracker. When the KCU receives the trigger, it fires a L1A and collects the data from the module ETROCs. The signal of the MCP is also later used for time reference during data analysis.

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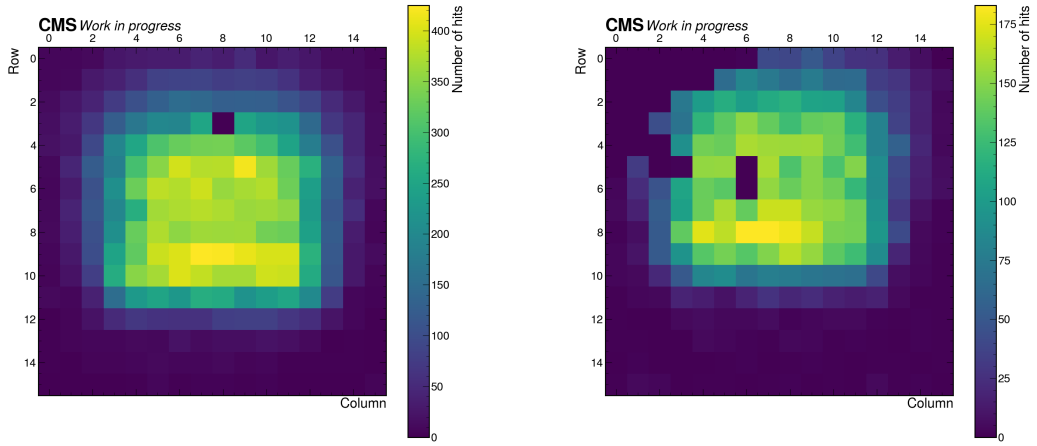

Figure 3: Number of hits collected per pixel for labeled ETL test modules 36 and 37 obtained during a run of the SPS test beam in May 2024.

4. Results

Preliminary results from the ETL test modules were obtained at two test beams conducted at the DESY (March 2024) and SPS (May 2024) facilities, using 6 GeV electrons and 120 GeV pions, respectively. Figure 3 shows two hit maps collected with two different modules labeled as 36 and 37, depicting the number of hits per pixel. These hit maps constitute the very first results obtained from the data collected in these test beam campaigns. The beam spot of the pion beam is clearly identified well over the noise, probing the capabilities of the full system DAQ chain. Future results will be presented from the full analysis with the data collected at both DESY and SPS.

References

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