PROCEEDINGS OF SCIENCE

Status of the ATLAS MDT Trigger Processor for the HL-LHC Upgrade

Adam Lux[a,*] **On behalf of the ATLAS TDAQ collaboration**

[a] *Boston University,*
590 Commonwealth Ave, Boston, USA

E-mail: ablux@bu.edu

The High Luminosity LHC (HL-LHC) will require upgrades to the ATLAS Level-0 (L0) muon trigger to cope with the increased collision rates. The Level-0 muon trigger will incorporate high precision hits from the Monitored Drift Tube chambers (MDTs) for the first time. The MDT Trigger Processor (MDTTP) uses the MDT hits to reconstruct muon tracks. This results in a reduction of the L0 trigger rate due to a sharpened efficiency turn-on curve, plus a rejection of combinatoric fakes. All MDT front-end electronics will be replaced during the HL-LHC upgrades necessitating new back-end electronics. The MDTTP will be used as the new MDT back-end. The MDTTP is an ATCA blade based on the Apollo platform. The 64 MDTTP blades also configure and monitor the MDT front-end electronics and read out MDT data for the final acquisition. An overview of the trigger algorithm and performance along with the status of the MDTTP hardware and firmware development and testing will be presented.

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1. Introduction

The current ATLAS L0 muon trigger, which uses hits from the Resistive Plate Chambers (RPC) in the barrel and Thin Gap Chambers (TGC) in the endcap, shown in figure 1, will be insufficient to handle the increased luminosity of HL-LHC. By including high precision hits from the MDTs to reconstruct tracks in the trigger, a significant reduction in the L0 trigger rate can be achieved. The MDTTP will be able to perform this track reconstruction. The MDTTP will be a set of 64 ATCA blades based on the Apollo platform [1] and will also be used as the new MDT back-end electronics.

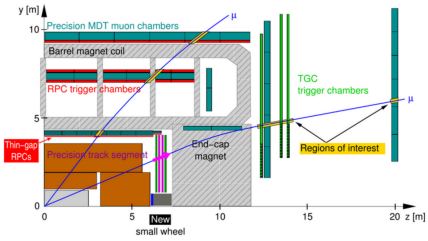
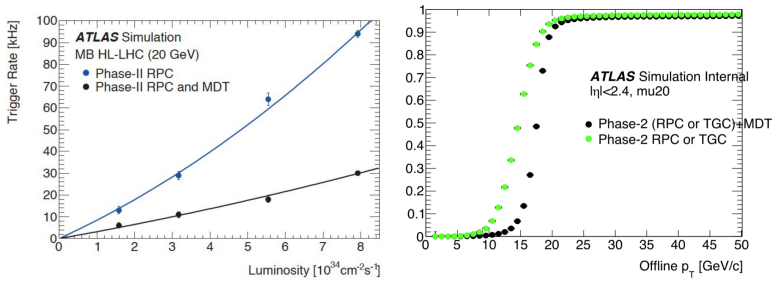


Figure 1: Cross section of the ATLAS Muon Spectrometer.

2. Performance Improvement

Muon trigger performance improvements due to the MDTTP include: increased rejection of fake muons, improvement of muon momentum resolution, and a sharper turn-on curve for the muon trigger, shown in figure 2b. These improvements lead to a reduction in the simulated L0 trigger rate by a factor of approximately 3 in the barrel and 6 in the endcap, see figure 2a.

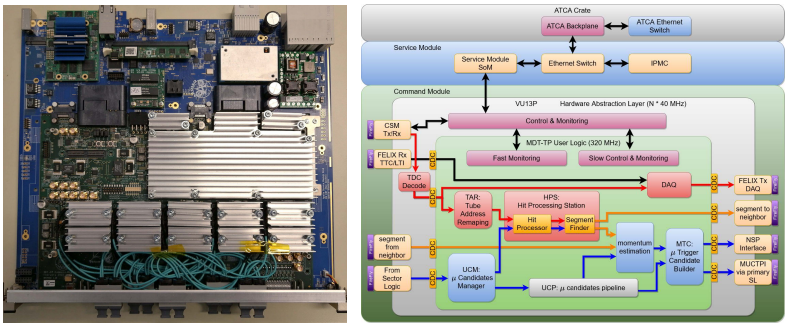


(a) **(b)**

Figure 2: Simulated trigger rate for the current and upgraded muon triggers vs luminosity (left) and simulated muon trigger turn on curves given the current and upgraded triggers (right) [2].

3. Prototype Hardware

The MDTTP prototype utilizes the open-source Apollo ATCA platform and consists of two boards: the Service Module (SM) and the Command Module (CM). The SM, shown in figure 3a as the blue outer board, is an application-agnostic module for all Apollo systems. It includes an



(a) **(b)**

Figure 3: Photo of the combined Service and Command Modules (left) and block diagram of the MDTTP firmware (right).

AMD Enclustra system-on-module (SoM), an ATCA Intelligent Platform Management Controller (IPMC), an Ethernet switch, and the power entry and management for the system. The CM, the green inner board shown in figure 3a, is application-specific and includes a VU13P Ultrascale+ FPGA, 10 Firefly optical transceivers, and a microcontroller unit for slow control and monitoring. Each Firefly has 12RX and 12TX fibers (24 fibers total) each of which can transmit at 14Gbps.

4. Firmware

The firmware for the MDTTP must be able to readout MDT hits, process 3 simultaneous track candidates in less than 1.8μs, and control and monitor the MDT front-end electronics. Communication between the MDTTP and the MDT front-end electronics happens via optical fibers, 2 uplinks and 1 downlink, between the MDTTP and the Chamber Service Module (CSM), which is the MDT front end. A block diagram of the MDTTP firmware and interfaces is shown in figure 3b.

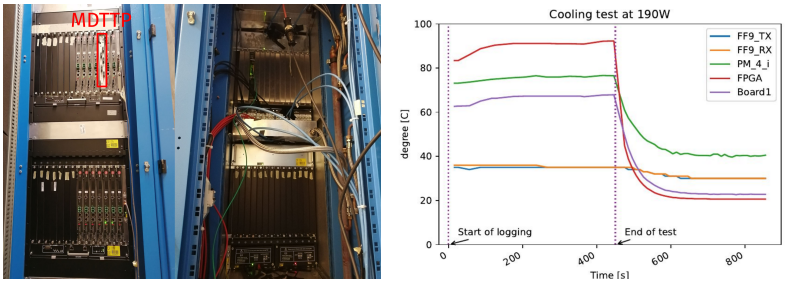
5. Trigger Algorithm

The L0 trigger selection is performed by the UltraScale+ FPGA. Triggers must be seeded by a candidate from the Sector Logic (SL). The firmware blocks associated with the trigger path are described as follows. First the firmware receives a muon candidate from SL. These seeds are either from the RPC or TGC. The Muon Candidate Manager (UCM) sorts the candidates from SL and processes the track angle and crossing position of the candidate for each MDT section. Next the MDT hits are filtered by the Hit Processor, which selects hits consistent with the position and beam crossing of the SL candidate. The Hit Processor also finds the drift radii of valid hits. In the next block, the filtered hits are reconstructed into segments via the Segment Finder (SF). Lastly the muon p_T is calculated from the reconstructed segments.

6. Prototype Validation

The MDTTP prototype has undergone a number of validation tests. The MDTTP to MDT front-end electronics connection was tested. Communication between the MDTTP and the lpGBT

of the front-end electronics was validated. The connection to the Front End Link Exchange (FELIX) [3] was tested with successful communication from both endpoints. Clock recovery and data transmission were also tested successfully. The thermal performance of the MDTTP has been tested at both CERN and MPI. The MDTTP was positioned between a number of heating blades (see figure 4a) to mimic other active MDTTPs. Power consumption was 190W at stable operation (see figure 4b). This test was performed using a specific endurance testing firmware with an active FPGA. During normal operation, power consumption is estimated to be <50W. The optical interface between the MDTTP and Sector Logic was tested using IBERT cores. Data transmission using fixed latency and test patterns was also verified from both ends.



(a) **(b)**

Figure 4: Photo of the MDTTP thermal testing setup at CERN (left) and a plot of the thermal tests results (right).

7. Current Development Status

All major interfaces to the MDTTP have been implemented and tested. These include CM-SM, FELIX [3], and CSM interfaces. The MDTTP firmware has been validated using a VHDL testbench along with the cocoTB framework [4]. HOG (HDL-on-Git) [5] is used for firmware code management. Firmware resource usage is well under 60%. A preproduction run of 16 MDTTP blades is set for next year. The SM and CM will be validated separately by the manufacturers, then the combined MDTTP blades will be tested at CERN by participating institutes.

References

[1] Apollo lhc documentation. https://apollo-lhc.gitlab.io. Accessed: 2024-09-26.

[2] J. Butler et al., *ATLAS TDAQ Phase-II Upgrade: Level 0 Muon MDT Trigger Processor Firmware Specification and Design.* Technical report, CERN, Geneva, 2022.

[3] The ATLAS FELIX Project. https://atlas-project-felix.web.cern.ch/atlas-project-felix/. Accessed: 2024-09-26.

[4] cocoTB. https://github.com/cocotb/cocotb. Accessed: 2024-09-26.

[5] Hog: HDL on git. https://hog.readthedocs.io. Accessed: 2024-09-26.