PROCEEDINGS OF SCIENCE

ATLAS upgrades

Yasuyuki Okumura on behalf of the ATLAS collaboration*

International Center for Elementary Particle Physics, The University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo, Japan

E-mail: yasuyuki.okumura@cern.ch

The ATLAS detector is undergoing preparation for major upgrades in order to get ready for the High-Luminosity Large Hadron Collider (HL-LHC) era, where higher luminosity and particle collision rates will present unprecedented challenges. This paper provides an overview of the upgrade projects, focusing on key areas including the Inner Tracking Detector (ITk), High Granularity Timing Detector (HGTD), calorimeter systems, muon system, and the Trigger and Data Acquisition (TDAQ) system. The ITk will fully replace the current Inner Detector with an all-silicon tracker, improving coverage and radiation tolerance. The HGTD will provide precision timing information to mitigate pile-up in the forward region. The calorimeter upgrades will involve new electronics for both the Liquid Argon and Tile calorimeters to cope with higher data rates. The muon system will be enhanced with new chambers and electronics for improved triggering. Additionally, the TDAQ system is being redesigned to handle increased event rates and larger data sizes. These upgrades are essential for maintaining ATLAS's performance in the high-intensity environment of the HL-LHC, ensuring its capability to explore new physics and further our understanding of the universe.

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*Speaker

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1. Introduction

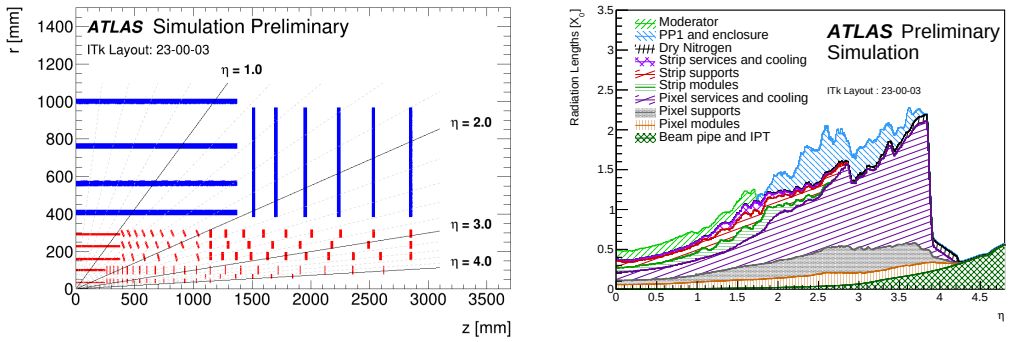
The High-Luminosity Large Hadron Collider (HL-LHC) is set to enhance the discovery potential for new physics by pushing the intensity frontier at the energy frontier. To adapt to the challenging environment during the HL-LHC operation, the ATLAS detector [1] is undergoing a substantial upgrade. This paper presents an overview of the major ATLAS upgrade projects planned for the next long shutdown (LS3) starting in 2026. The key areas of upgrade include the Inner Tracking Detector (ITk), High Granularity Timing Detector (HGTD), calorimeter electronics, muon system, trigger and data acquisition (TDAQ) system, and forward detectors.

2. Inner Tracking Detector (ITk)

The current Inner Detector of ATLAS will be completely replaced by the new all-silicon Inner Tracking Detector (ITk), designed to handle the high particle densities expected at HL-LHC.

2.1 ITk Overview

The ITk will consist of silicon pixel and strip sensors, with a total silicon area of 13 m^2 for the pixel detector and 168 m^2 [2] for the strip detector [3]. The ITk provides full tracking coverage up to $|\eta| = 4.0$ with at least nine silicon layers along individual trajectories with finer segmentation (Figure 1(a)) and with lower material budget (Figure 1(b)). The ITk is expected to provide excellent tracking efficiency (Figure 2(a)), typically greater than 90%, while reducing combinatorial backgrounds (Figure 2(b)) owing to optimization of reconstruction algorithms and the optimal ITk layout.

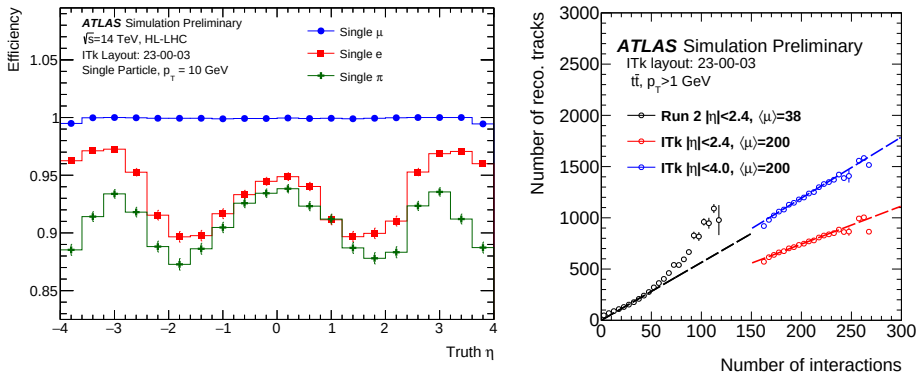


(a) **(b)**

Figure 1: (a) A schematic illustration of the ITk system, where the components of the strip detector are depicted in blue, and those of the pixel detector are depicted in red. (b) The material distribution within the ITk volume is shown in radiation lengths (X_0) as a function of pseudorapidity (η) [4].

2.2 ITk Pixel System

The pixel system [2] is divided into inner, outer, and endcap regions, each with different pixel sizes of 25×100 μm^2 in the innermost barrel and 50×50 μm^2 elsewhere. It will feature more



(a) **(b)**

Figure 2: (a) Tracking efficiency for individual particles with $p_{\mathrm{T}} = 10$ GeV is shown for muons, electrons, and pions, without pileup effects. (b) The number of reconstructed tracks per event with $p_{\mathrm{T}} > 1$ GeV is displayed for $t\bar{t}$ events, with an average of 200 pileup collisions, as a function of the actual number of interactions. For comparison, results are shown for the Run-2 detector geometry using the Run-2 legacy reconstruction software [4].

than 1.4 billion channels in total. The innermost layers will use 3D sensors, while the remaining layers will rely on planar sensors. Additionally, the inner pixel system is designed to be replaceable, mitigating radiation damage over the course of the HL-LHC operation.

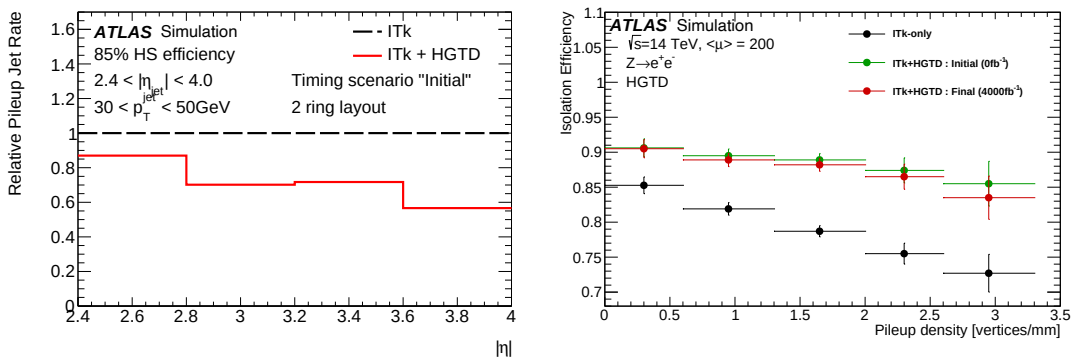
2.3 ITk Strip System

The strip detector [3] consists of a four-layer barrel and two six-layer endcap disks, covering up to $|\eta| = 2.7$ with 18,000 modules. Each strip is approximately 75 μm wide, and the system features 60 million channels. Current status includes progress in sensor production and successful thermal cycle tests for the modules, with assembly of large global mechanics underway at CERN (Figures 3)

Figure 3: Assembly of the outer cylinder started in June 2024 (left). The Strip Layer 3 cylinder also arrived at CERN for insertion inside the outer cylinder. The first insertion tests have been performed successfully in July 2024 (right).

3. High Granularity Timing Detector (HGTD)

The High Granularity Timing Detector (HGTD) [5] is a novel detector that will be installed between the ITk and the endcap calorimeter to mitigate the pile-up effects at HL-LHC with precise timing measurements. The addition of precise timing information for individual tracks will allow ATLAS to distinguish between activities from different collisions that are spatially close but temporally separated within a bunch crossing with finite bunch length. The HGTD will provide a hit-level timing resolution of around 70 ps and a track-level resolution of 30–50 ps in the forward region ($2.4 < |\eta| < 4.0$), where spacial vertex separation is more difficult. The HGTD will use Low-Gain Avalanche Detectors (LGAD) to achieve this performance, contributing not only to pile-up jet suppression but also to improve the selectivity of track-based lepton isolation owing to additional suppression of tracks from pileup collisions with timing information (Figures 4).



(a) **(b)**

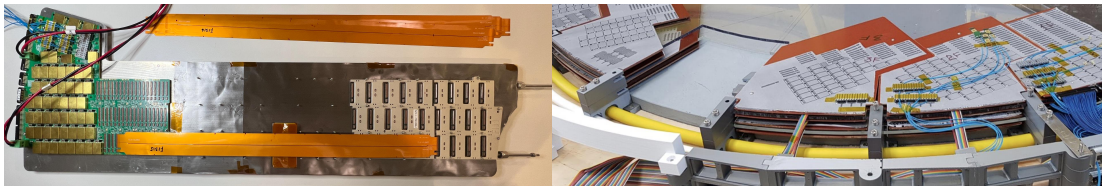
Figure 4: (a) Relative rate of pileup jets as a function of jet pseudorapidity (η) for jets with $30 < p_{\mathrm{T}} < 50$ GeV. (b) Efficiency for electrons to meet track isolation criteria as a function of local vertex density, comparing the ITk-only and ITk+HGTD configurations.The plot shows performance for two timing resolution scenarios, representing the beginning and end of HL-LHC operation [5].

Production is advancing with the pre-production of ASICs and hybridization of LGAD sensors showing promising results. The first prototype of the Peripheral Electronics Board (PEB) is being tested in an assembled demonstrator, where system-level integration tests are also progressing well (Figure 5(a)). A careful assessment of assembly with mock-up has been done to ensure a smooth installation during the LS3 (Figure 5(b)).

4. Calorimeter Upgrades

4.1 Liquid Argon (LAr) Calorimeter

The LAr calorimeter [6] will undergo significant electronics upgrades to handle the increased data rates of the HL-LHC. Continuous readout at 40 MHz with a total bandwidth of 345 Tbps is being developed, supported by new high-precision front-end electronics. The LAr Signal Processor, responsible for waveform feature extraction, will host approximately 33,000 links at 10 Gbps. Production of LAr-specific ASICs is already in progress, with successful prototype tests for both front-end boards and off-detector electronics.



(a) **(b)**

Figure 5: (a) Assembled demonstrator used for system-level integration tests. (b) Mock-up setup for validating installation methods.

4.2 Tile Calorimeter

The Tile Calorimeter [7] will also see an overhaul of its electronics, including a new digital trigger system and higher data bandwidth for 40 MHz readout. Reassembly and upgrade of photomultiplier tube (PMT) blocks are part of the upgrade, including replacement of the most radiation-exposed PMTs and the development of new front-end mainboards. A demonstrator system has already been installed in ATLAS and is currently collecting data, with final design efforts for off-detector electronics ongoing.

5. Muon System Upgrade

The muon system [8] will be upgraded to improve triggering capabilities and cope with the higher particle flux at HL-LHC. The barrel inner station will see new resistive plate chambers (RPCs) added and small-diameter monitored drift tubes (sMDTs) replacing the existing drift tubes in the barrel's small sectors. The endcap inner station will be upgraded with triplet thin gap chambers (TGCs). As of June 2024, sMDT production is complete, and new TGC sectors are set to be installed during the Year-End Technical Stop (YETS) of 2024–2025. A "dry run" campaign for the electronics installation is already underway to validate the installation scheme in the LS3. Electronics demonstrators are currently operational during the Run-3 data-taking in the ATLAS cavern to demonstrate the communication to the frontend electronics as well as the monitoring of single event upset rate on the FPGA (Figures 6).

6. Trigger and Data Acquisition (TDAQ)

The TDAQ system upgrade [9] is critical to meet the data demands of HL-LHC. The Level-0 (L0) trigger will operate at a rate of 1 MHz with a 10 μs latency, and the Event Filter (EF) output rate will be 10 kHz. The estimated event size is 4.6 MB. Prototyping and testing are ongoing for both the L0 trigger and data acquisition system (Figure 7), with successful communication tests between subsystems already conducted.

The event filter demonstrators are progressing well, particularly in integrating support for GPUs and FPGAs into ATLAS software. By 2025, these efforts will provide crucial input for final hardware decisions, ensuring a scalable and efficient system [10].

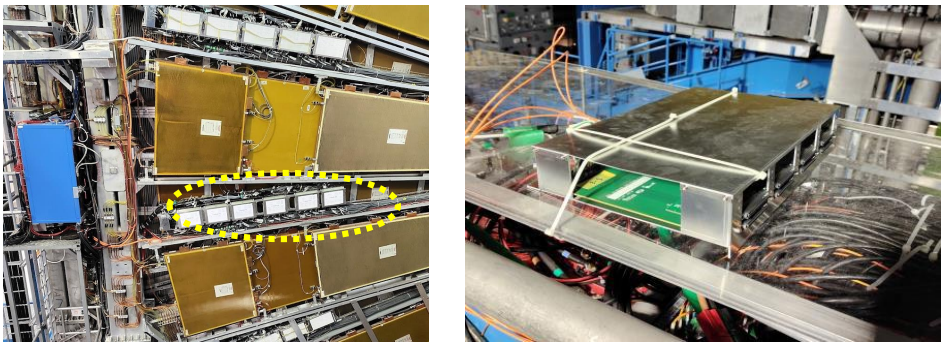


Figure 6: Photographs showing the demonstration of actual installation of phase-2 frontend electronics for TGC, including board placement and cablings (left), and electronics demonstrators installed in the ATLAS cavern (right) to validate communication links and measure the single event upset rate on the FPGA during Run-3 operations.

Figure 7: Photographs of prototypes for the Level-0 Muon Trigger Sector Logic electronics in ATCA form factor (left) and the FELIX PCIe card for the readout in the Phase-II system with extended input bandwidth (right) [9].

7. Conclusion

The ATLAS detector upgrades are essential for the successful operation of the HL-LHC. The introduction of the ITk and HGTD will improve tracking and pile-up rejection capabilities, maximising the physics potential even in high-intensity environments of HL-LHC. The calorimeter and muon system upgrades will introduce new trigger and readout electronics to cope with higher collision, increasing the performance, especially the selectivity in the trigger stage. The TDAQ system is also evolving to cope with the unprecedented data rates of the HL-LHC. As the production phase advances, testing and integration efforts are ramping up, with major components already arriving at CERN. The full installation is scheduled to begin after the completion of Run 3, positioning ATLAS to continue delivering groundbreaking results well into the HL-LHC era.

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