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ATLAS Liquid Argon Calorimeter Front-end electronics Phase-2 upgrade

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A new era of hadron collisions will start around 2029 with the High-Luminosity LHC, which will allow to collect ten times more data than the amount that has been collected during the past 10 years of operation at LHC. This will be achieved by higher instantaneous luminosity, at the price of higher number of collisions per bunch crossing. In order to withstand the high expected radiation doses and the harsh data taking conditions, the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded. The electronic readout chain is composed of four main consituents. New front-end boards and calibration boards will be installed on-detector, while, off-detector, signal processing boards and a new timing and control system will take care of the energy and time reconstruction and synchronization of the readout electronics respectively. The custom electronics in each subsystem will satisfy stringent requirements for both noise level and linearity, and, for the on-detector components, maintain functionality up to 1.4 kGy (TID) and 4.1×10^{13} n_{eq}/cm^2 (NIEL). The current development status and the performances of both the on-detector and off-detector electronics will be presented.

The Eleventh Annual Conference on Large Hadron Collider Physics (LHCP2023)
22-26 May 2023
Belgrade, Serbia

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1. The ATLAS Liquid Argon (LAr) Calorimeter

The ATLAS Liquid Argon (LAr) calorimeter [1, 2, 3] is a system of sampling calorimeters, relying on cryogenically-cooled liquid argon as active medium. It measures the energy, position, and timing of electromagnetic showers initiated by the interaction of incoming electrons, photons, and jets, produced by proton-proton (pp) collisions with the detector material, by relying on its four components. The Electromagnetic Barrel (EMB) and the two Endcaps (EMEC) provide precision EM calorimetry in the pseudorapidity regions $|\eta| < 1.475$ and $1.375 < |\eta| < 3.2$ respectively, while full azimuthal coverage is reached by arranging the layers of active and absorber material (lead) in an accordion-shaped geometry. The Hadronic Endcaps (HEC) use copper layers as passive material and cover the $1.5 < |\eta| < 3.2$ range, while the Forward Calorimeter (FCal) (relying on tungsten or copper plates as absorbers) extends the pseudorapidity coverage in the region $3.2 < |\eta| < 4.9$. The EMB and EMEC are longitudinally segmented into three layers, termed "front", "middle", and "back". An additional layer, termed "presampler", is placed before the front layer in the region $|\eta| < 1.8$. The calorimeters are segmented in cells with varying granularity in both the η and ϕ directions, amounting to a total of 182,468 read-out channels. The read-out electronics sample the signal from the calorimeter cells at 40 MHz (corresponding to the frequency of the bunch-crossing at the interaction point), and sends the digitized pulses off-detector for triggering and further processing.

2. The High-Luminosity LHC phase

The Run 4 of the LHC, expected to start at the end of a three year-long shutdown (LS3) in 2029, will open the High-Luminosity (HL) LHC data-taking season, during which the LHC is foreseen to deliver an enormous amount of data, corresponding to an integrated luminosity of 3000 fb^{-1} in a 10-year period (until around 2041). This will by achieved by the LHC providing instantaneous luminosities up to 7 times the design value (up to 7×10^{34} $\text{cm}^{-2}\text{s}^{-1}$), corresponding to 200 simultaneous pp interactions per bunch crossing (i.e. pile-up), where the average value for Run 2 (Run 3) is 33.7 (65). In order to survive the extreme HL-LHC environment, the ATLAS detectors will undergo major upgrades, termed Phase II upgrades, that are expected to be completed during LS3. The Phase II upgrade also involves the read-out electronics of the ATLAS LAr calorimetric system [4], which, in his current form, would not be able to cope with the challenges of the HL-LHC data-taking. In particular, the new electronics will have to be compatible with the upgraded ATLAS Trigger and Data-Acquisition systems (TDAQ) [5] - designed to accomodate the high data volume at the HL-LHC - and tolerate the stronger expected radiation doses, while still retaining an excellent efficiency and performance for the measurement of electrons, photons, and jets.

3. The LAr Phase II upgrade

The read-out electronics for the LAr calorimeter are organized in on- and off-detector components, all outlined in Figure 1. Signals from the calorimeter cells are read out by the Front-End Boards (FEBs), that are placed directly on the cryostats that house the LAr calorimeter. The second generation of the FEB, named FEB2, performs analog processing of the calorimeter signals, including amplification, CR-$(\text{RC})^2$ shaping, and splitting in two overlapping gain scales (Low an High). Both gain scales are

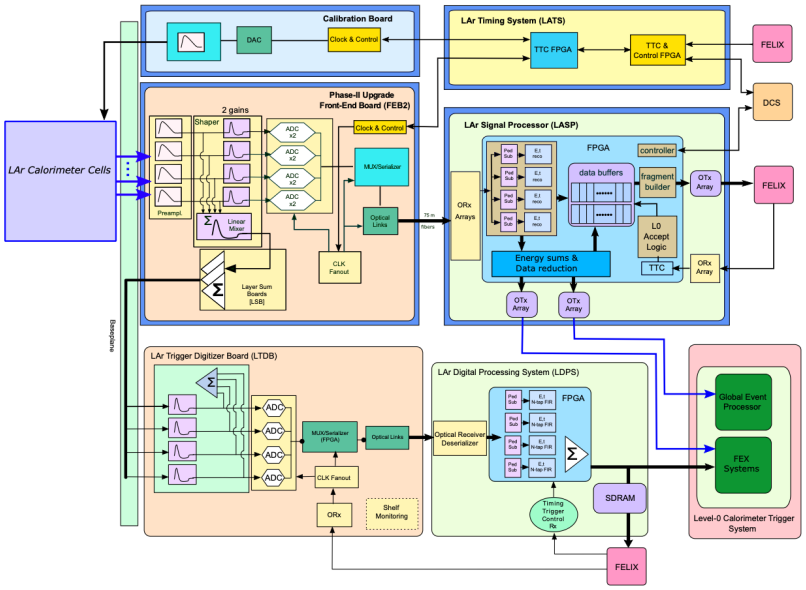

Figure 1: Architecture of the LAr calorimeter read-out electronics in Phase II.

digitized directly on the FEB2s. The digital signals from each calorimeter cell are sent via optical links to the LAr Signal Processor Boards (LASPs), which perform digital filtering, and an accurate energy and timing calculation via FPGAs. The LASPs send inputs to the trigger systems, and data is buffered until a trigger decision is reached. Upon a trigger accept, data is sent to the DAQ chain. A second read-out chain, complementary to the one described above, exploits directly the FEB2 analog signals to provide summed cells input to the digital trigger installed in "Phase I" (outlined in the bottom of the diagram in Figure 1). This involves, on-detector, the LAr Trigger Digitizer Board (LTDB) and, off-detector, the LAr Digital Processing Board (LDPB). A complete description of the Phase I trigger (that will remain operational during the HL-LHC stage, complementary to the Phase II system) is provided in [6, 3].

3.1 Front-end electronics

3.1.1 Front-End Boards

The amplification, shaping, and digitization of the calorimeter signals on the FEB2s requires several custom ASICs, installed directly on the board. The ALFE, based on 130 nm CMOS technology, will be the custom Pre-Amplifier/Shaper (PA/S) on the FEB2. Tests on the current prototype (the ALFE2) revealed a very low non-linearity (< 0.1%), as well as low equivalent noise input of < 350 nA for 10 mA channels. Radiation testing also show that the ALFE2 maintains a good performance after a 12-kGy dose, corresponding to 8 times the expected threshold (1.4 kGy). Both gain scales from the PA/S output are digitized with a > 11 bit precision at 40 MHz by the COLUTA Analog-to-Digital Converter (ADC), a 16-bit custom ASIC designed in 65 nm CMOS technology. The integration of the custom ASICs with the full LAr read-out chain is tested with a FEB2 pre-prototype, termed "slice test board". This corresponds to 1/4 of the final board and has demonstrated the functionality of the read-out and control for 32 channels (PA/S plus ADCs plus lpGBT optical links). The slice test

board was also used for testing the new power distribution system on the board: a single 48-V power supply is converted to lower voltages (namely, 1.2 V and 2.5 V) using custom DC-DC converters. Coherent noise levels are under control using radiation-soft solutions, while further tests are foreseen for radiation-hard DC-DC converters (based on the CERN-developed bPOL48V and bPOL12V) as well as for the new full-size FEB2 prototype.

3.1.2 Calibration boards

The calibration of the FEB2 is performed by injecting a known ionization-like signal in the read-out electronics. Two custom ASICs, installed on the Calibration boards, are used for generating the calibration pulses: the CLAROC, designed on 180 nm HV SOI CMOS XFAB technology in order to cover the full 16-bit dynamic range, and the LADOC (a 16-bit Digital-to-Analog Converter based on TSMC 130 nm technology). Tests on the current prototypes (namely, CLAROCv4 and LADOCv2) demonstrated that the two custom ASICs meet both linearity and uniformity requirements (non-linearity < 0.1%, and non-uniformity < 0.25%), while tests on radiation hardness are ongoing.

3.2 Off-detector electronics

3.2.1 LAr Signal Processor (LASP)

The LASPs are installed off-detector, and each of them receives the fully digitized data from 8 FEB2 boards at the LHC clock frequency of 40 MHz: in total, the off-detector electronics receive 345 Tbps of data at 10 Gbps. The digital filtering of the input signals, the determination of the calibrated cell energies and signal times with respect to the bunch crossing time (including an active correction of out-of-time pile-up) is performed by two Intel Agilex FPGAs. These are installed on an ATCA-compliant board (namely, the LASP main blade), interfaced with a Smart Rear Transition Module (sRTM). The functionality of the power distribution and the FPGA configuration has been validated on a testboard. Further tests aim to optimize the resource usage and the power consumption of the FPGAs and validate the integration with the FEB2.

3.2.2 LAr Timing System (LATS)

The LAr Timing System (LATS) handles the Trigger, Timing and Control (TTC) distribution, configuration, and monitoring of all the 1524 FEB2 and 122 Calibration boards in the LAr system, by relying on lpGBT protocol. This is achieved by the LATOURNETT board, that is equipped with 13 AREA Cyclone 10 FPGAs. The development of the firmware as well as integration tests with the central ATLAS TTC system are ongoing.

4. Conclusions

The Phase II upgrade of the ATLAS LAr calorimeter was presented. For the Phase II upgrade, expected to be completed during the LS3, the read-out electronics are being re-designed to cope with the harsher data-taking conditions expected at the HL-LHC. Major progress was reached for the design and testing of both the on-detector (FEB2 and calibration boards) and the off-detector (LASP and LATS) components: tests on the custom ASICs show promising results on linearity, uniformity, noise, and radiation-hardness (on the front-end side). Further production and integration tests are foreseen during the Run 3 data-taking period, before the installation in the ATLAS cavern.

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