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Calibration of the CROC_v1 pixel chip for the CMS Phase-2 Inner Tracker

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The Compact Muon Solenoid (CMS) detector is currently advancing with its Phase-2 upgrade, in preparation for operation in the High-Luminosity LHC. Once upgraded, the CMS experiment will incorporate a completely new tracker, including an Inner Tracker based on pixellated silicon sensors. The pixel chips for the Inner Tracker are developed by the RD53 collaboration.

In this paper, we present the latest calibration test results for the RD53B-CMS (CROC_v1) chips with sensors. The performance of the chip is studied in order to optimize the calibration procedure for the real experiment. Using the latest DAQ system features, test results to optimize the hit detection threshold and signal gain using the chip's internal calibration circuit and a radioactive X-ray source, are presented.

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1. The High-Luminosity LHC

The High-Luminosity LHC (HL-LHC) [1] is planned to start operation in 2029, with greatly improved physics potential compared to the current LHC. It should reach the instantaneous luminosity of 7.5×10^{34} cm^{-2} s^{-1}, 7.5 times greater than the nominal LHC luminosity of 10^{34} cm^{-2} s^{-1}. This will be achieved by increasing the number of proton-proton (pp) collisions (pile-up) to 200, compared to an average of 52 today. The CMS experiment is expected to collect an integrated luminosity of 3000-4000 fb^{-1} over 12 years of running.

The CMS and ATLAS experiments are preparing for their Phase-2 upgrades aimed at delivering the best possible performance under HL-LHC conditions. Compared with the initial version of the CMS detector, the upgraded detector will have to operate optimally with ~8 times the number of tracks, ~7.5 times higher trigger rate (100 kHz to 750 kHz at the Level 1 trigger), and ~12 times higher radiation dose (100 Mrad at the innermost layers to 1.2 Grad).

2. The CMS Phase-2 Tracker

The CMS experiment is working on a completely new silicon tracker detector for the Phase-2 upgrade [2]. The upgraded tracker will consist of two major parts: the Inner Tracker and the Outer Tracker. The Outer Tracker will make use of silicon strip and silicon macro-pixel sensors and tracking information will be used in the CMS Level 1 trigger for the first time. The Inner Tracker will consist of very high-granularity silicon pixel detectors, discussed in the next section. A schematic view of the Phase-2 Tracker is shown in Fig. 1.

3. The Phase-2 Inner Tracker

The Inner Tracker design has been developed to fulfil requirements dictated by CMS physics goals. Pixel size will be reduced from the current 150×100 µm^2 to 25×100 µm^2 to improve track resolution and reduce occupancy. The sensor active thickness will also be reduced from the current 285 µm to 150 µm. Two different sensor technologies will be used: 3D pixel sensors in Barrel layer 1 (brown in Fig. 1) with planar n-in-p pixel sensors everywhere else. The Phase-2 Inner Tracker will have 12 forward disks instead of the current 3 and will increase the geometric acceptance from

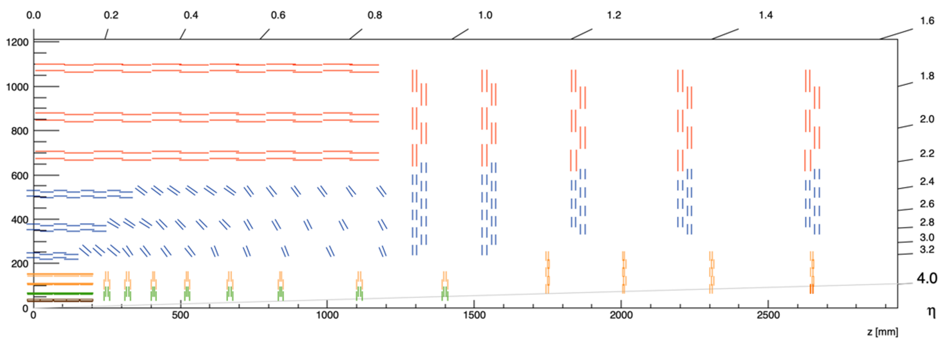

Figure 1: A one-quarter slice of the CMS Phase-2 Tracker in $r-z$ [2]. The red and blue lines show the modules of the Outer Tracker, while the yellow, orange, green, and brown lines denote the modules of the Inner Tracker.

Figure 2: A CROC_v1 chip (under the transparent cover) mounted on the single-chip card (green).

$|\eta| < 2.5$ to $|\eta| < 4.0$. In total, the Inner Tracker will comprise around 2 billion pixels. The whole Inner Tracker is designed for simple installation and removal which allows for replacing damaged or inefficient parts during short stops.

The pixel detectors will use radiation-hard readout chips, designed by the RD53 Collaboration – a joint effort between CMS and ATLAS. These chips are designed to be radiation tolerant up to 1 Grad. Currently, the 2$^{\text{nd}}$-generation prototype chips RD53B-CMS, called CMS ReadOut Chip or CROC_v1 are undergoing intensive testing [3]. A single-chip card with a CROC_v1 chip is shown in Fig. 2. A new data acquisition and control software, called Ph2_ACF is developed to perform system tests and production quality assurance for both Inner and Outer Tracker systems.

4. Threshold tuning

The threshold of each pixel in a chip is determined by a combination of three registers: the global threshold, the pixel's individual threshold trimming register (TDAC), and the global register LDAC_LIN which determines the TDAC strength. Fig. 3 shows the distribution of thresholds before and after TDAC tuning while keeping the average threshold at 1500 electrons of signal. The results show that TDAC tuning can reduce the dispersion (standard deviation) of thresholds down to ~40 electrons of signal. This is two times better than what was achievable with the RD53A demonstrator chip, which had 4 instead of 5 bits for threshold trimming. A comparison between RD53A and CROC_v1 of the best possible threshold spreads at different LDAC_LIN values can be seen in Fig. 4. Systematic tests show that the threshold dispersion is not correlated with the global threshold value. This is demonstrated in Fig. 5, where threshold dispersion changes by less than 10% when the global threshold is changed by 40% and TDAC values are not retuned.

5. Gain tuning

Signal strength is measured by counting the number of 25 ns clock cycles the signal spends above the threshold (time-over-threshold or ToT), up to a maximum value of 14 allowed by the 4-bit register size (up to 31 when using 6-to-4-bit compression). The preamplifier feedback ("Krummenacher") current can be tuned using a global register to obtain different signal gain curves. This allows one to choose between better resolution or a larger dynamic range. Gain curves obtained without using 6-to-4 bit compression are shown in Fig. 6. ToT response has been observed to become linear when the Krummenacher current value is <60 (in DAC units) or when charges are significantly larger than

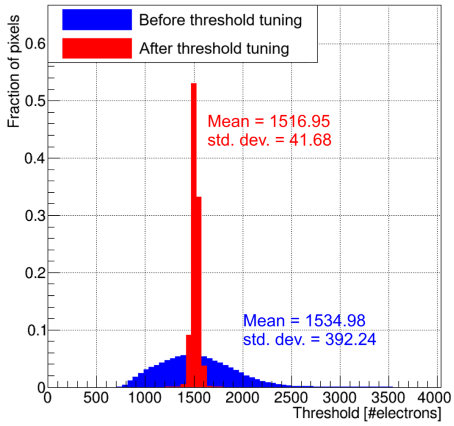

Figure 3: Threshold distribution on a tested chip. The blue (red) colour shows the distribution before (after) TDAC tuning.

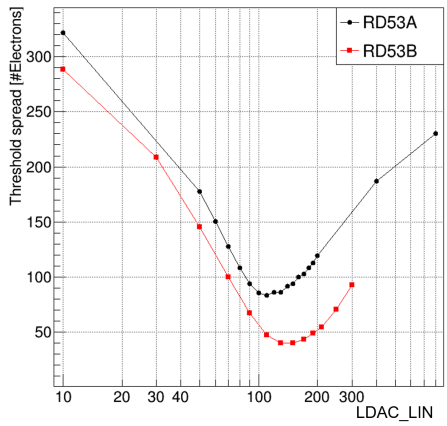

Figure 4: A comparison of threshold dispersions between RD53A (black) and CROC_v1 (red) chips at different LDAC_LIN values.

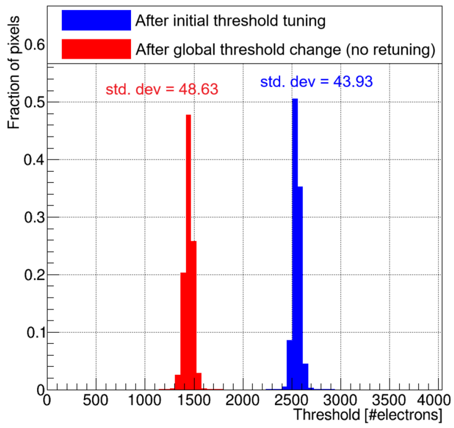

Figure 5: Threshold distribution before (blue) and after (red) changing the global threshold while keeping TDAC values the same.

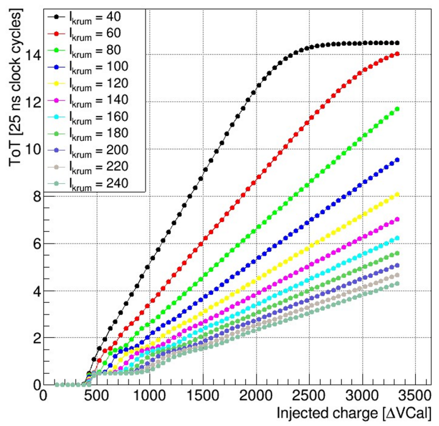

Figure 6: Time-over-threshold dependence on injected charge. Different curves correspond to different Krummenacher current values (in DAC units).

the threshold, which is the intended behaviour [4].

6. Threshold calibration

The threshold of each pixel is measured by injecting calibration pulses of known amplitude into the front-end. The calibration pulse strength (and consequently the threshold) is measured in DAC units, called ΔVCal. The physical value of ΔVCal, expressed in electrons, has been measured in two ways: using the chip's internal voltage multiplexer (VMUX), and using a radioactive monochromatic ^{241}Am X-ray source. The measurement results using VMUX are shown in Fig. 7. The results show that 1 ΔVCal is approximately equal to 4.93 electrons of charge. The measurement using the X-ray source was made to provide a second measurement, independent of the calibration circuit. ^{241}Am emits 59.54 keV photons and is expected to create 16268 electron-hole pairs per photon, assuming that the energy required to create an electron-hole pair in silicon is 3.66 eV [5]. The signal distribution (in ΔVCal units) of the registered hits is shown in Fig. 8. Comparing the position

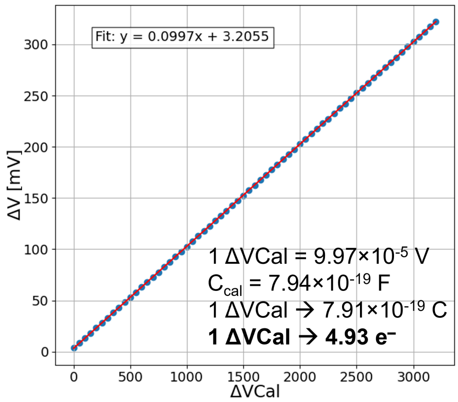

Figure 7: Calibration voltage measured via the voltage multiplexer (VMUX) as a function of the ΔVCal DAC value.

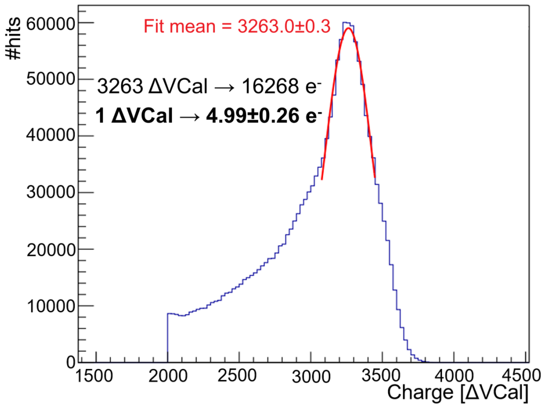

Figure 8: Signal distribution of the registered ^{241}Am X-ray hits. Only single-hit clusters are considered. Signal is measured in ΔVCal units.

of the maximum with the expected number of electrons, the ΔVCal value has been estimated to be equivalent to 4.99 ± 0.26 electrons. The two measurements were shown to agree within errors, thus 5 electrons of charge is a good approximation for one ΔVCal unit.

7. Summary

A new tracker is in preparation for the CMS Phase-2 upgrade, featuring high radiation tolerance and high granularity – a significant improvement over the current tracker. The pixel detector chips for the Phase-2 Inner Tracker are developed by the RD53 collaboration, with the second-generation prototype (CROC_v1) undergoing intensive testing. Our chip performance tests show good results: (a) two times smaller threshold spread compared to the RD53A demonstrator chip, (b) the signal gain response behaves as intended by the chip designers [4], (c) two different measurements of the calibration voltage unit agree well within errors. As the studies of the CROC_v1 continue, the design for the final chip iteration, CROC_v2, has already been submitted and is currently in the final stages of validation before entering the production phase.

References

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