PROCEEDINGS OF SCIENCE

Performance and characterisation of the Phase-2 CMS Inner Tracker Endcap pixel detector

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The High Luminosity Large Hadron Collider (HL-LHC) at CERN is expected to collide protons at 14 TeV center-of-mass energy and to reach the unprecedented peak instantaneous luminosity of 7.5 $\times 10^{34}$ cm^{-2}s^{-1} with 200 collisions in average per bunch crossing. This will allow the ATLAS and CMS experiments to collect integrated luminosity up to 4000 fb^{-1} each during the project lifetime. To cope with this extreme scenario, the CMS detector will be substantially upgraded before the HL-LHC phase, a plan known as the CMS Phase-2 upgrade. The entire CMS Inner Tracker (IT) detector will be replaced, and the new detector will feature increased radiation hardness, higher granularity, capability to handle higher data rates and longer trigger latency. The upgraded IT will be composed of a barrel part, TBPX, and small and large forward disks, TFPX and TEPX. The novel scheme of serial powering will be deployed to power the pixel modules, and new technologies will be used for a high bandwidth readout system. The TEPX detector has four large disks on each end, extending the tracking coverage up to $|\eta| < 4.0$. Each disk employs a thin PCB which carries the data and power from/to the modules. In this contribution, the design of the new TEPX detector will be presented, focusing on the disk characterization. The performance of the CMS Read-OUT Chip (CROC) quad modules, either digital or with planar sensors, will be discussed, with a focus on the comparison between the behaviour standalone or in a TEPX disk serial power chain, in terms of noise and threshold uniformity. The final design of the TEPX disk PCB is evaluated by testing the modules connected to the disk, in terms of data transmission quality compared to the standalone case.

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1. The Phase-2 Upgrade of the CMS Inner Tracker

The HL-LHC run will collide protons with peak luminosity 7.5×10^{34} cm^{-2}s^{-1} with 200 collisions in average per bunch crossing, delivering up to 4000 fb^{-1} integrated luminosity to CMS and ATLAS each. The Phase-2 upgrade of the CMS Inner Tracker project [1] aims at building a new inner tracker detector with improved radiation hardness, higher granularity, longer trigger latency and capability to handle higher data rates for the HL-LHC phase. The Tracker Endcap Pixel (TEPX) detector has four disks covering the tracks up to $|\eta| < 4.0$. TEPX implements quad modules, with planar sensors bump-bonded to the CMS ReadOut Chips (CROC) in 65 nm CMOS technology [2]. The read-out chips for CMS have been developed by the RD53 Collaboration [3], with two different subsequent versions. The first one, the RD53A, has three different analog sections, while the second one, the RD53B, or CROC v1, features only the linear analog FE, and it has the same size as the final read-out chip. These proceedings include the characterization of RD53A and RD53B modules on prototype TEPX disks.

2. Serial Powering of the Pixel Modules

The tracker in the current detector uses parallel powering for the pixel modules. However, given the higher number of channels in the Phase-2 detector, implementing parallel powering would result in a large number of cables and increased material budget. Therefore, the Phase-2 inner tracker employs serial powering of pixel modules, connecting up to 11 modules per chain. The modules in serial powering are required to be electrically insulated with respect to the underlying mechanical structure, because they have different local grounds inside the chain. The pixel chips use current shunts and low-dropout (LDO) regulators [1], referred to as shunt-LDO, to ensure constant current sharing among the four chips that are powered in parallel in each module. As the first implementation of serial powering in high energy physics for large systems, the electrical performances of the inner tracker prototypes need to be tested in details.

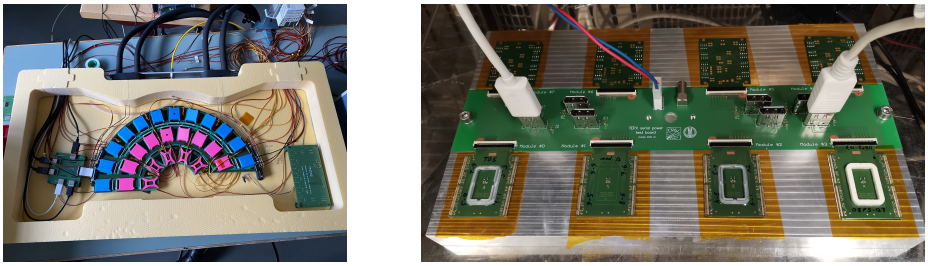
3. Performance Tests of 2×2 Pixel Chip Modules in a Serial Powering Chain

The electrical and thermal performances of 2×2 pixel chip modules RD53A and RD53B are performed in serially powered chains. The testing setups are shown Figure 1(a) and Figure 1(b) for the RD53A and RD53B modules, respectively.

3.1 RD53A Modules in a Disk PCB with CO_2 Cooling

The RD53A sensor modules are tested in a disk PCB, glued to a mechanical structure composed of a carbon foam core, with two carbon fiber sheets outside. The pipes of the CO_2 cooling system run inside the carbon foam (Figure 1(a)). During these tests, the CO_2 temperature was -20 °C. The modules are operated in serial power with a constant current of 6.2 A. The data is read out through the lines in the PCB, and then a flex cable connecting the disk to an adaptor board. Display port cables then are used up to the FC7 DAQ system [5].

The chips in all modules are tuned to a threshold of 2000 e. An S-curve is obtained by measuring the hit efficiency while increasing the injected charge. The threshold is defined as the charge where

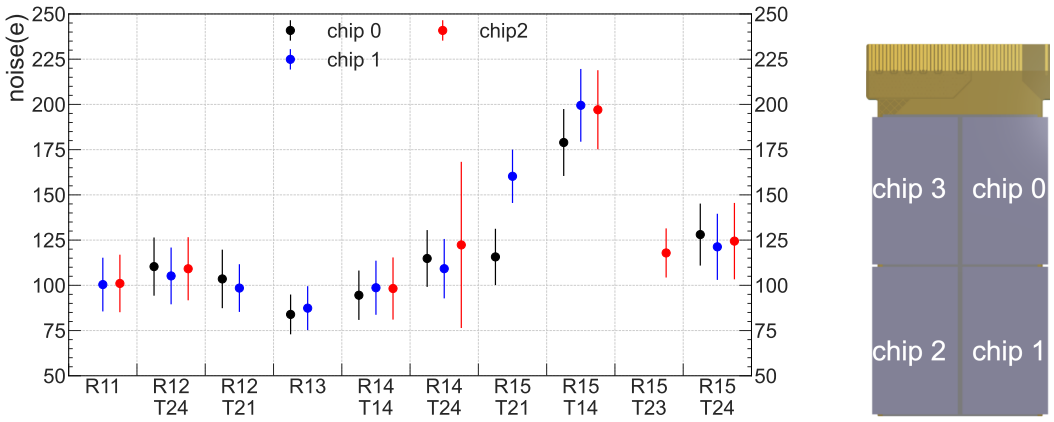


(a) **(b)**

Figure 1: (a) The prototype TEPX half-disk with 5 RD53A modules installed in the innermost ring. The prototype disk PCB is placed on the mechanical structure composed by an internal layer of carbon foam, sandwiched between two sheets of carbon fiber. The pipes of the CO_2 cooling system run inside grooves in the carbon foam layer. The setup is placed inside a cooling box with continuous blowing of dry air. (b) The RD53B modules installed in the TEPX serial power test board and placed inside a climate chamber.

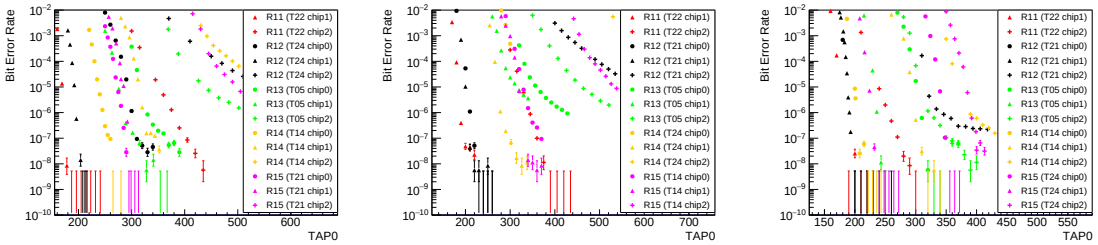
the efficiency is 50% and the noise as the difference in the values of the charges corresponding to 70% and 30% of the efficiency. The collection of S-curves for all the functional chips are measured to extract the threshold and noise distributions of the pixels in the chips. Figure 2(a) shows the mean and standard deviation of the noise distributions for these chips. In this prototype version of disk PCB, we are able to read out 3 (chip 0, 1 and 2 in Figure 2(b)) out of 4 chips for each module in the innermost ring. Comparing the performances of the modules T21, T14 and T24 at different positions, we observed higher noise levels at the position R15, which is the position with the longest data line within in the disk PCB. The values of the module noise for the other positions are around 100 e, and they are similar to the values measured in a different board in the stand-alone mode. Different ground configurations for the disk mechanics have been tried, but position R15 still results in a higher value of the noise. Preliminary measurements in the new version of the disk PCB with RD53B modules show that the noise is instead constant over the five positions of R1. Tests of the new PCB after gluing it to the disk mechanical structure will be performed in 2024 to exclude the interference of the underlying carbon fiber on the performance of the disk PCB.

In the test of the data read-out performance, the bit error rate is scanned in the available range of the "TAP0" parameter (the `CML_TAP0_BIAS` register of the RD53A chip [4]), which modulates the signal amplitude. Figure 3 shows the testing results of three setups. In Figure 3(a) and 3(b), all the setups are the same expect the positions of the modules. In Figure 3(a), a shorter flex cable is used than that in the other figures. The bit error rates are positively correlated with the data transmission distance. As shown in Figure 1(c), the position R11 is the closest to the flex cable, thus has the shortest data transmission line and the lowest bit error rate, while R15 on the opposite side has the longest data transmission line and highest bit error rate. The error rates of the chip 2 is higher than the other chips for all the modules in all the tests. The comparison of Figure 3(a) and (b) indicates that the modules have minor effects on the bit error rate. Figure 3(c) shows lower bit error rates than the other setups, especially in chip 2, indicating the improvement of the data transmission quality from a shorter flex cable with less impedance mismatch.



(a) **(b)**

Figure 2: (a) The noise of all the functional chips of the RD53A modules in the innermost ring of the prototype half-disk. The centers of the data points represent the mean of the noise distribution and the error bars represent the standard deviations. The R11-R15 correspond to the 5 positions in the ring from left to right in Figure 1(a). T14, T21, T23 and T24 are the names of different modules, among which T21 and T23 has parylene coated on the backside, while T14 and T24 do not have coating. (b) The positions of the chips in an RD53A module.

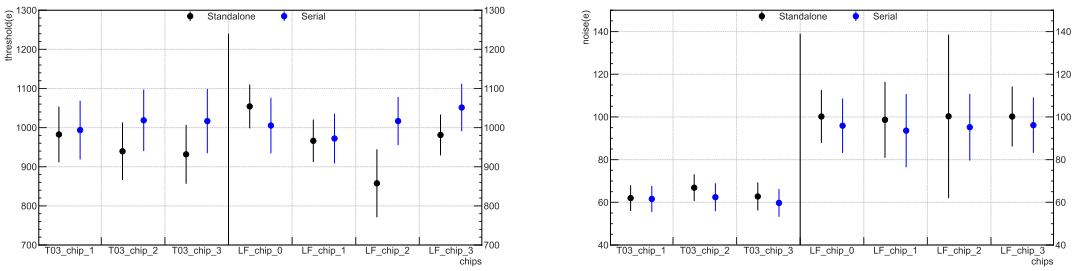


(a) **(b)** **(c)**

Figure 3: The bit error rate of the visible chips in the RD53A modules in the 5 positions of the innermost ring. (a) and (b) are comparisons of swapping the modules in different positions. (c) is measured with a shorter flex cable than that in (a) and (b).

3.2 RD53B Modules in a Serial Powering Chain

The RD53B modules have been tested in a serial power test board, cooled down in a climate chamber to −35 °C (Figure 1(b)). The board has been designed on purpose for the first characterization of the RD53B chips in serial power before the new version of the disk PCB becoming available. Figure 4 shows threshold and noise of a digital module (T03) and a module with LFoundry silicon sensors (LF) in standalone tests and serial powering extracted from similar S-curve scans to those in Section 3.1. The module performances are similar in standalone and serial powering tests in terms of threshold and noise levels. The LF module has slightly higher noise levels than the T03 module as expected, because of the additional noise introduced by the sensor.



(a) **(b)**

Figure 4: The means and standard deviations of the threshold and noise distributions for a digital module (T03) and a module with LFoundry silicon sensors (LF) in either standalone test or serial powering. (a) Threshold tests; (b) noise tests.

4. Summary

The RD53A and RD53B modules are tested in a serial power chain to validate the electrical performance of the CMS inner tracker in the Phase-2 upgrade. The RD53A modules are tested in a prototype half disk of TEPX and cooled down with pipes filled with a mixture of liquid and gas CO_2. The noise test shows a dependence on the position in the ring. The bit error rates are affected by the module position because of the data line length and the flex cable design. The positions of the chips in the module can also influence the bit error rates. The RD53B modules are tested in a serial power test board. The noises and thresholds of the modules in serial powering are similar to the standalone results. The sensor modules have higher noise levels than the digital modules.

References

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