PROCEEDINGS OF SCIENCE

The LHCb Mighty Tracker

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The LHCb detector is set to undergo a significant upgrade during the upcoming long shutdown 4 of the LHC. This upgrade will result in a nearly tenfold increase in instantaneous luminosity, reaching $1.5{\times}10^{34}$ cm^2 s^{-1}, with an integrated luminosity expected to rise from 50 fb^{-1} to 300 fb^{-1}. To effectively handle the elevated track densities, the downstream tracking stations will employ silicon pixel sensors in the inner region where particle fluences are highest. The MightyPix ASIC is a Monolithic HV-CMOS sensor based on the HV-MAPS families MuPix and ATLASPix, specifically designed to meet the requirements of LHCb. The Mighty Tracker silicon detector will covering an extensive active area of 18 m^2 will comprise over 2×10^9 pixels. The first iteration of the chip, along with its features and design are presented. Notable recent advances in the mechanical and electronic design of the silicon modules are also shown. Progress on prototyping developments, which focus on simulation, verification and FPGA emulation work are outlined. The latest beam test campaigns have yielded valuable insights into the radiation performance of precursor chips of the MightyPix. Noteworthy highlights are presented, accompanied by plans in place to maximise the chip's performance.

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1. Introduction

The Large Hadron Collider Beauty detector [2][3] is a flavour physics detector, designed to detect decays of b- and c-hadrons for the study of CP violation and rare decays. In Long Shutdown 4 of the LHC, the detector will be installed and commissioned the second upgrade of the experiment [1], with the goal of significantly increasing its data taking capability. The peak instantaneous luminosity will increase to $1.5 \times 10^{34}\,\mathrm{cm}^2\,\mathrm{s}^{-1}$ to fully exploit the High Luminosity LHC. In order to meet this luminosity requirement, the granularity of all detector components will be increased. Furthermore, the new components must be more radiation tolerant due to the ensuing increase in particle flux.

The tracking stations for LHCb Upgrade I, known as Sci-Fi, consist of six layers of scintillating fibres. To cope with the increased pile-up in Upgrade II, the inner section of the Sci-Fi will be replaced with a silicon pixel detector. This new detector, combining both pixel and fibre elements is titled Mighty Tracker (MT). This paper focuses on the new inner pixel layers of MT.

2. The Mighty Tracker Pixel Detector

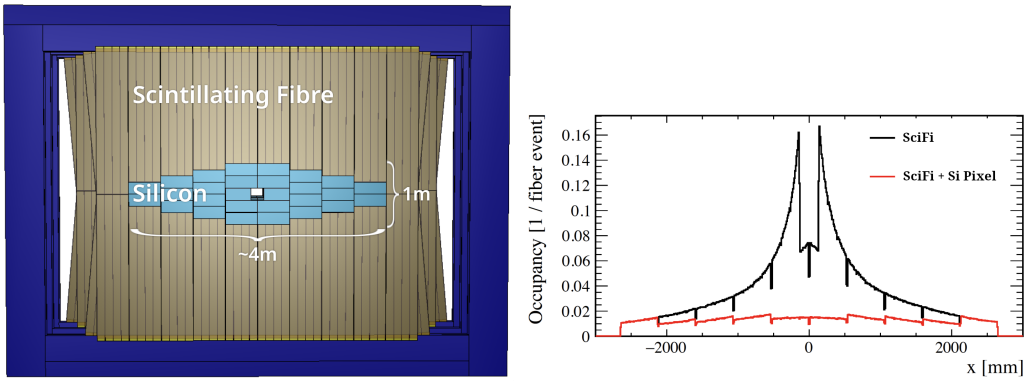

Figure 1: **L**: Mighty Tracker: the outer region shows the scintillating fibre tracker, and the inner region (blue) shows the silicon pixel layer. **R**: The occupancy of the scintillating fibres without and with the silicon layer.

The Mighty Tracker is required to be (1) low-mass: to minimise the number of secondary particles produced by detector interactions; (2) cooled below 0°C: to minimise detector aging; (3) have good spatial resolution: to provide adequate particle track reconstruction.

Fig. 1L shows the Mighty Tracker design geometry and dimensions. The total silicon area is approximately $18\,\mathrm{m}^2$. The increased luminosity and radiation damage in Upgrade II would significantly degrade the tracking performance of Sci-Fi to 50%. Fig. 1R shows that the addition of the pixel layer greatly improves the performance by reducing the occupancy in the fibres to a manageable level.

2.1 MightyPix

The Mighty Tracker design centres around a new pixel ASIC - the MightyPix. It is based on the ATLASPix[4] and MuPix[5] family of chips, using the TSI 180 nm process. The ASIC is a

HV-CMOS design [6] with sensor and readout circuit on the same silicon die. The chip is required to have a pixel size less than 100 µm × 300 µm, an in-time efficiency of greater than 99% and a radiation tolerance of 6×10^{14} MeV · n_{eq}/cm^2.

The first version of the chip (MightyPix1) has been produced this year (shown in Fig. 2). The chip is 200 µm thick and approximately 2 cm × 0.5 cm in size. As such it has full column length of the final design but only one quarter width. The full design is segmented in four identical column readout regions, and so results from testing the one quarter width MightyPix1 are expected to have negligible difference to the full size chip. Full compatibility with the LHCb timing and control system are not fully realised in MightyPix1. These features are planned for the second version of the chip.

At the time of write testing had only begun on MightyPix1. Preliminary testing shows major features are working including, but not limited to, configuration and readback, timing synchronisation, resetting, low speed data readout. These initial results are promising; and the chip will be taken for beam tests in 2024 where the required chip performances for Upgrade II will be studied.

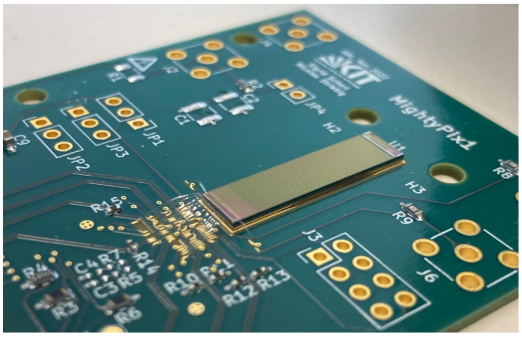

Figure 2: MightyPix1 wire-bonded to a PCB for testing. *(Photograph courtesy of Karlsruhe Institute of Technology.)*

3. Detector & Module Design

The Mighty Tracker consists of six layers of silicon planes. Each layer is composed of 28 modules. The modules have two variants - long and short. There are only two short modules per layer, situated left and right of the LHCb beam pipe. The module are populated front and back to make best use of the available space (see Fig. 3). Power dissipation in the sensor region is expected to be ~150 mW/ cm^2.

Prototype module substrates are being developed at the University of Manchester, to investigate assembly procedures and measure cooling performance. Fig. 4 shows an example of carbon fibre and carbon foam substrate samples. X-ray tomography is used to check for inconsistencies in the produced samples.

4. Electronics and Readout

The modules employ CERN radiation hard components for the electronics design. These include the low power GigaBit Transceiver (lpGBT) [7] and Versatile Link Plus components[8]. In

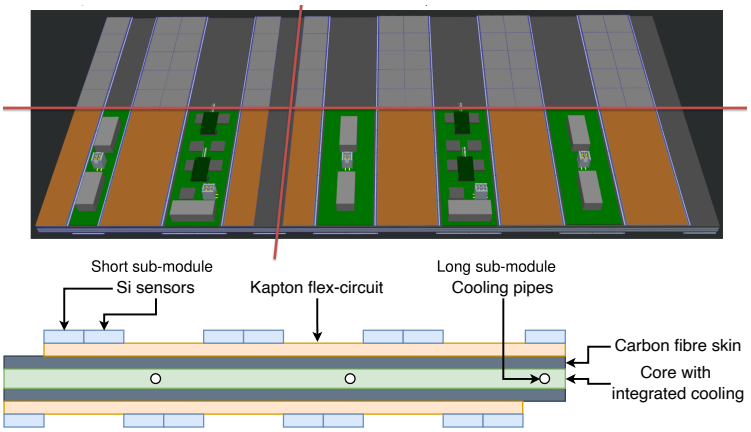

Figure 3: T: Current design of the inner short modules. The modules are sub-divided into sub-modules. **B**: Module cross-section.

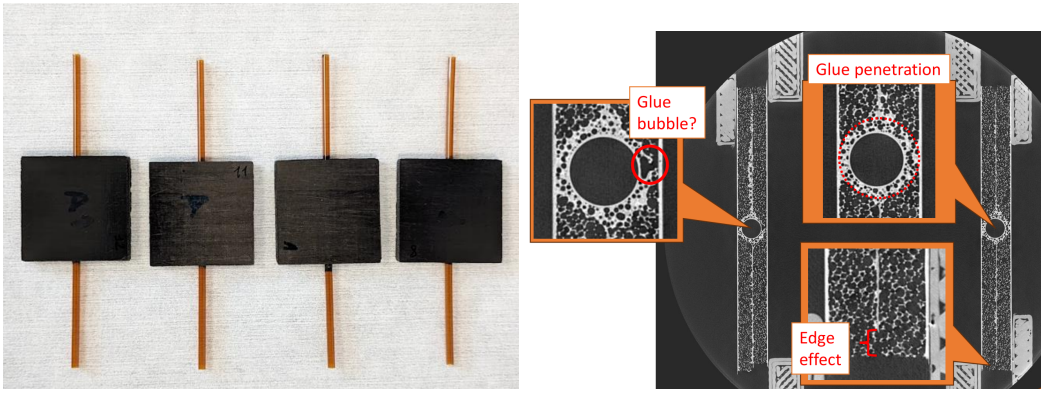

Figure 4: L: Prototype carbon-foam substrates **R**: X-ray tomography of substrate samples (*(pictures courtesy of U. Manchester).*

the baseline design DCDCs [9] are used for powering both the MightyPix and the other components on the modules. However, given power requirements and space constraints, Serial Powering [10] is strongly being considered for Mighty Tracker. This has the added advantage of reducing the material in the detector acceptance.

Due to the higher particle flux in the innermost region of the detector, the modules near the beam pipe require more readout capability than those on the exterior of the detector. Monte-Carlo simulations at Upgrade II luminosities have been prepared, and studies have been performed to determine the bandwidth as a function of detector geometry [11]. The number of electronic and optical links and their speed required for each module is being optimised. The innermost MightyPix require four links at 1280 Mb/s whilst the outermost only require one link at 320 Mb/s.

In order to catch potential digital design problems with MightyPix, several design strategies have been employed. A verification framework has been developed to test the conformity of MightyPix to the LHCb timing and fast control system, and to test the bandwidth limitation of the chip (results are described in the next section). An chip emulator is under development using an FPGA to mimic the behaviour of the MightyPix1. The code for the digital design of the chip has

been ported to FPGA, and a configurable data generator has been added in place of the analogue components. An Enclustra Mercury KX1 has been used for the FPGA. A carrier board has been developed at University of Bonn for prototyping the MightyPix. This is connected to a Versatile Link Demonstrator Board (VLDB+)[12] with an lpGBT. In this manner, communication between the lpGBT and emulated MightyPix can be tested, including timing, control and output data at different rates. The same carrier board will be used to test the initial versions of MightyPix. This allows functional tests to be carried out prior to chip resubmission.

The VLDB is also used to test communication with the backend electronics. Currently a Xilinx KCU105 FPGA Evaluation board is used for testing the readout chain. lpGBT firmware is being ported to the Intel FPGA platform which is used in LHCb. These systems can be adapted to test the signal integrity of data from the MightyPix in the first module designs.

5. Performance studies

The MightyPix verification framework has been used to measure how the chip performs at high data rates. The maximum expected hit rate for MightyPix1 chips closest to the beam line is 17 MHz/ cm^2, as estimated using LHCb simulation. Poisson distributed data normalised to match different LHCb data rates has been fed into a model of the pixel matrix, and the output of the model is compared to measure the efficiency. Fig. 5 show the efficiency as a function of hit rate. The efficiency stays above 99% above the maximum hit rate. Improvements to the remaining inefficiency are under development for MightyPix2 and outlined in an upcoming paper [13].

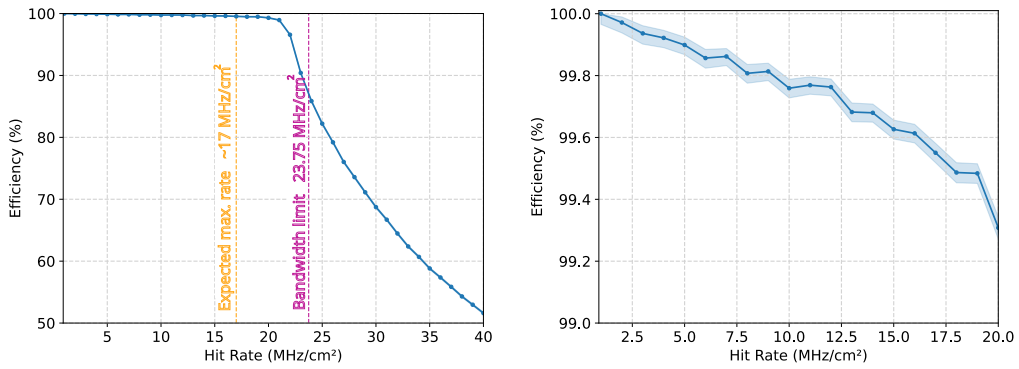

Figure 5: **L**: Simulated MightyPix1 readout efficiency vs. hit rate The expected maximum rate of 17 MHz/ cm^2 and maximum available bandwidth of 20 MHz/ cm^2 are indicated by vertical lines **R**: A zoomed view showing the small efficiency loss above 99%.

The ATLASPix 3.1 has been under study in advance of the MightyPix. This is the closest full size chip in the HV-CMOS family. It has a pixel size of 50 µm × 150 µm and a chip size of 2 cm × 2 cm, both of which are similar to the final MightyPix design. The amplifier and comparator of the chips are different so similar timing resolution is not expected. The primary interest in studying ATLASPix 3.1 is to determine its radiation hardness.

Beam tests were performed at the DESY Testbeam Facility in December 2022. Tests were performed at temperatures: 10, 0, and 5°C; and with three different irradiated samples: unirradiated,

1×10^{14} MeV $\cdot$ $n_{eq}/cm^2$and 3×10^{14} MeV $\cdot$ n_{eq}/cm^2. Fig. 6 shows the noise (dashed lines) and the efficiency (solid lines) as a function of pixel hit threshold (in DAC counts). The ideal scenario in this plot is to have a working threshold where both the noise remains low and the efficiency remains high even under higher irradiations. In all cases but one, a threshold above 140 DACs would keep the noise at a manageable level. However, the efficiency drops significantly above 140 DACs in all cases; and it is worst at higher radiation doses. It is also clearly desirable to keep the chips at lower temperature as performance suffers above 0°C. The design requirement for the MightyPix is 6×10^{14} MeV $\cdot$ n_{eq}/cm^2, so the radiation tolerance needs a clear improvement for MightyPix. More detail on these results is given in [14].

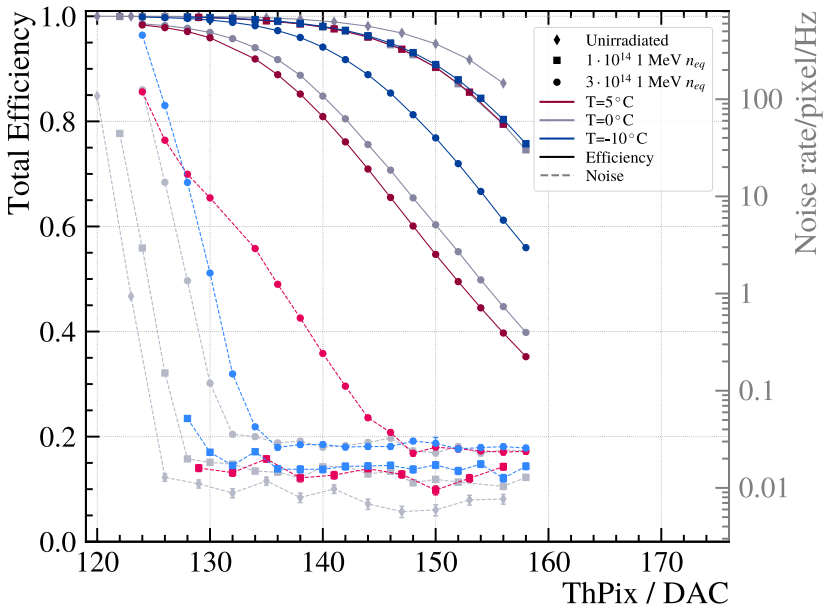

Figure 6: ATLASPix 3.1 efficiency and noise as a function of pixel hit threshold (in DACs). Details are described in the text.

6. Conclusion

Progress in many aspects of the Mighty Tracker design has been shown. The electronic and mechanical designs are evolving and prototypes for the module design are being produced and studied. CERN radiation hard components are being used where possible and optimisations have been made to limit the necessary number of readout channels. The first version of the MightyPix has been produced and will be studied in detail in the next year, with improvements for the second version already well underway in order to meet the full LHCb specifications. Simulation, verification and emulation techniques are being employed to find issues in advance of chip submission. Results from predecessors of MightyPix indicate that radiation performance is critical to meet the design requirements.

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