PROCEEDINGS OF SCIENCE

The next generation cameras for the Large-Sized Telescopes of the Cherenkov Telescope Array Observatory

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PoS(ICRC2023)740

The latest generation of silicon photomultipliers (SiPM) offers twice as much sensitivity to Cherenkov light observed at ground level when compared to photomultipliers. Their use for imaging atmospheric Cherenkov telescopes is increasing, from the FACT telescope, the pioneer, to the small-sized telescopes of the Cherenkov Telescope Array (CTA) or the LHAASO WFCTA camera. The robustness of the SiPMs represents a unique opportunity to ensure long-term operation with low maintenance. In this work, we present the latest developments and performance of a SiPM camera aiming at upgrading the large-sized telescopes (LST) cameras of CTA. The SiPM camera, equipped with 0.05 deg pixels, provides images of improved resolution for better feature extraction. The increase in the number of pixels has driven the development of low-power front-end electronics whose design is presented in this work. We also present the fully digital readout architecture of the proposed camera, which will enable the implementation of novel triggering algorithms based on artificial intelligence.

38th International Cosmic Ray Conference (ICRC2023)
26 July - 3 August, 2023
Nagoya, Japan

1. Introduction

The Cherenkov Telescope Array (CTA) represents a significant leap forward in the field of gamma-ray astronomy, promising unparalleled sensitivity and performance. As part of this ambitious project, a series of Large-Sized Telescopes (LSTs) are being constructed at the Observatorio del Roque de los Muchachos, with completion scheduled for mid-2025. The LSTs are designed to meet the stringent requirements set forth by CTAO and enhance the array's capabilities in studying gamma-ray sources across a wide range of energies.

The first LST (LST-1 [1]) boasts a remarkable 23-meter diameter parabolic reflective surface. This reflective surface, encompassing an area of 400 m^2, efficiently focuses Cherenkov light onto a sophisticated camera system. The camera employs cutting-edge photo-multiplier tubes, which convert the incoming light into electrical signals, ready for subsequent processing by dedicated electronics. Furthermore, the LST-1 with an impressive height of 45 meters and weighing approximately 100 tonnes, possesses exceptional agility, capable of repositioning itself between any two points in the sky within a mere 20 seconds.

This rapid response time ensures the capture of elusive low-energy transient gamma-ray signals. With its large collecting area, the LST-1 provides unprecedented sensitivity to gamma rays at the lowest energies, making it an indispensable component of the CTA.

The collective efforts of the LST Collaboration will result in the construction of three additional telescopes with overall completion slated for 2025 - will follow a commissioning period where all four telescopes will be operated in stereoscopic mode improving significantly the sensitivity of the system.

The effort shall, however, not stop here as Cherenkov cameras have a life-cycle of 15 years while the Observatory shall deliver scientific data for at least 30 years. It is therefore a necessity to foresee the replacement of those Cameras as a great opportunity to upgrade their performance. The two main changes that the proposed camera will adopt with respect to the existing one are the use of silicon photo-multipliers (SiPMs), instead of photo-multiplier tubes (PMTs), and a fully digital readout as opposed to a readout based on analogue memories. The reasons for these choices are detailed in the following sections.

2. Camera design choices

2.1 Focal plane instrumentation

2.1.1 Light guides

SiPMs seem not to be the perfect photo-sensor for the Cherenkov camera application.

One of their main drawbacks is its increased sensitivity above 540 nm, where the night sky background flux increases significantly.

A higher rate of background photons increases the chances of pile-up effects and forces to increase the operational threshold.

Some Cherenkov cameras featuring SiPMs have tackled this issue by applying a coating onto the camera entrance window which reflects the photons with up to 90% efficiency above 540 nm [5, 7].

However, because of the sheer size of the LST entrance window, applying such coating layer is not a feasible solution. Even if few companies or institutes in the world may have a vacuum chamber large enough to realise the coating on a monolithic window, the result would be highly non-uniform. The intended solution to segment the entrance window into several smaller pieces was also discarded as it impacts both the mechanical stability and the photon distribution on the photo-sensing plane.

In addition to the size, the material of the entrance window matters. For instance, the entrance window of the LST-1 camera is made out of Shinkolite PMA[1] [8] that provides excellent transparency down to 280 nm and, once moulded to a specific shape, offers as well, great mechanical properties. However, the application of a dichroic optical filter requires reaching high temperatures which would entail both optical and mechanical properties of this material. The alternatives are as well not satisfactory: borofloat glass has a cut-off at 300 nm and quartz is too fragile to be produced in large sheets.

Having discarded the possibility to perform the coating on the window, applying such coating on the mirrors directly was also envisaged. However, a factor of ten on the single mirror coating cost combined with the large number of mirrors mounted on the LST dish (198) makes this solution too expensive..

Eventually, considering the technological challenge and the cost increase, adapting the coating of the light guides seems to be the best solution to cut-off wavelengths above 540 nm. This is being studied and presented in [10]. The solution will only be so efficient as a fraction of the light will go straight to the sensor without hitting the light guide, but the high compression factor achieved for this pixel size (nearly factor 6), makes the solution very appealing and undoubtedly the simplest to be deployed on such large cameras.

2.1.2 SiPM

Since 2019, Hamamatsu Photonics K. K. (HPK) has been developing a prototype sensor with properties optimised for Cherenkov imaging cameras. The key characteristics for the optimisation were the enhancement of the sensitivity toward UV light, a reduction of the correlated noise and a short time response.

The core technology is the S13360 or better known as low cross-talk technology. HPK modified the micro-cell design to increase significantly the photo-detection efficiency below 300 nm, matching very well the Cherenkov spectrum. In [6], Annexe , we can derive that the current telescope has an efficiency of 14.8% for the Cherenkov spectrum from 200 nm to 1000 nm while the telescope equipped with the S13360-XX75-UVE SiPMs would reach 30.9%. On the other hand, the efficiency of background light detection goes from 1.6% to 8.6%. Eventually, the signal-to-noise ratio (SNR) is 1.17 for the PMT against 1.05 for the SiPMs. This difference imposes very strict requirements on the design of the pre-amplifying stage. It is of utmost importance that pre-amplifying ASIC provides a single photon response with a full width at half-maximum smaller than 3 ns. Such a short response is required to limit the impact of background photons piling up and eventually mimicking a potentially relevant physics signal. As for the size and shape of the sensor, the baseline is still

[1] https://www.m-chemical.co.jp/shinkolite/index.html

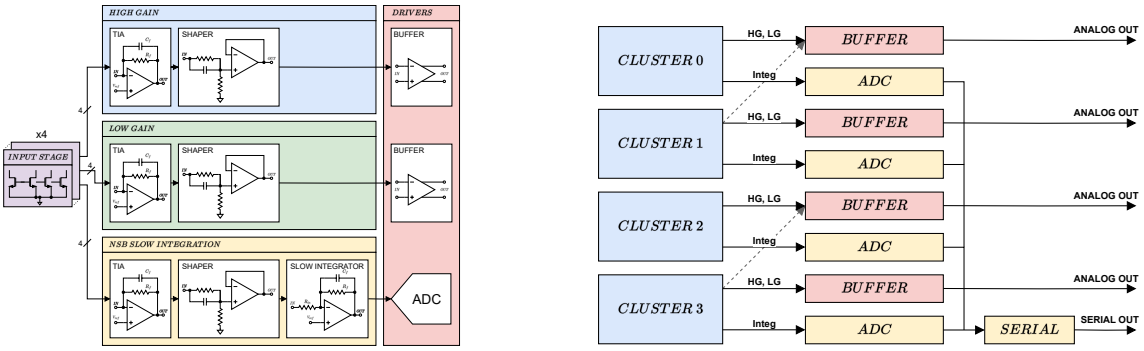

Figure 1: Left: preliminary readout of a pixel (four channels) of the PRESSEC ASIC. As visible on the right diagram, the ASIC includes four of these clusters.

to use sensors of ∼1 cm^2, similar to the one in [7], divided into four channels. More about the characterisation of this prototype sensor can be found in [11].

2.2 Front-end electronics

2.2.1 Pre-amplifying stage

The pre-amplifying stage will be implemented in an application specific integrated circuit (ASIC) and is being designed by a collaboration of institutes: the University of Geneva (CH), the University of Barcelona and Polytechnic University of Catalonia (ES). The ASIC architecture has already been decided (Fig. 1). It features a current-mode input stage with high-performance current mirrors to feed three paths: the high-gain, the low-gain and the current slow integration used to monitor the level of night sky background (NSB) by adjusting accordingly the working point of the sensor. The high and low-gain paths will feature a summation stage implemented as a trans-impedance amplifier and a shaping stage. Finally, the output drivers are optimised for fast analogue to digital converters.

Due to the large number of pixels, the goal is to achieve the performance requirements with a single readout electronics chain per pixel. Because the signal are constantly digitised with fast analogue to digital converters (FADC), the power consumption and the cost are strong limitations for an alternative solution. In this case, only the high gain will be used to provide the best charge resolution for faint events. The performance goals are a dynamic range of 250 p.e. for a SNR > 5. Preliminary simulations of the design show that this cannot be reached, consequently, a compromise between the dynamic range and the SNR will have to be made.

The reduction in dynamic range will only slightly impact the performance as shown in [3, 7, 12]. When the pre-amplifying stage saturates, the signal amplitude reach a maximum but the charge continue to increase however losing its linearity. A proper signal integration allows to maintain the charge resolution requirements and the event can still be fully exploited for physics analysis. The decision to add a low-gain path is then twofold: it allows the cross-calibration of the response of the high-gain path through a programmable selection of the output and it offers, to the ASIC, a broader range of users by increasing the linearity of the response up to more than 1000 p.e..

The ASIC is being designed in TSMC 65 nm CMOS technology and a first version will be submitted by the end of Summer 2023 to characterise and validate the output drivers. By the end

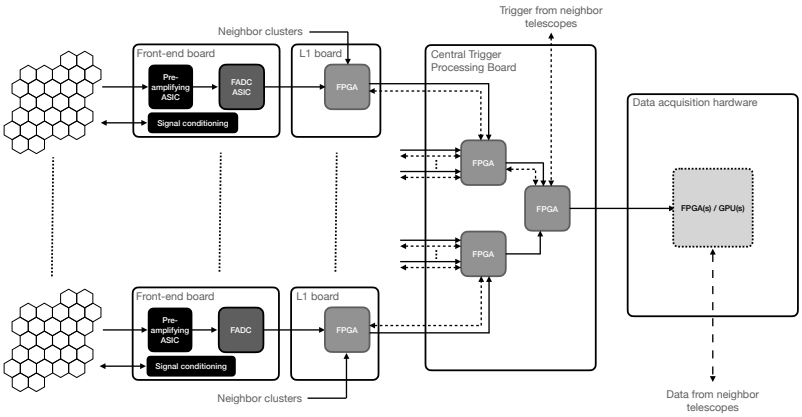

Figure 2: Simplified diagram of the readout architecture. The number of links and their speed is not shown as still under discussion. The synchronisation and clock signals are not displayed but are critical to the system. The shape of the pixel cluster is not representative of the final one.

of Winter 2024, the first complete prototype ASIC will be submitted.

2.2.2 Fast Analogue to Digital Converter (FADC) ASIC

The FADC converts the analogue input into a 12 bits digital code at a rate of 1 GSps. In order to achieve the desired performance within a reasonable cost in terms of area and power consumption, an architecture comprising a combination of pipeline and time-interleaving techniques was devised. Contrary to the conventional pipeline approach where each stage converts the amplified residue of the preceding one in a sequential way, the proposed architecture employs a parallel configuration where all the stages work on the same input sample. The comparison thresholds of each stage are adjusted according to the conversion result of the preceding stage. The first stage is a regular 3 bits flash ADC. The second stage is a combination of three time-interleaved 3 bits flash ADCs with controlled thresholds. The third stage is a combination of 16 6 bits successive-approximation register ADCs. The second and third stages use lower sampling frequencies together with progressive time-interleaving factors to ensure sufficient time for the conversion without affecting the overall sample rate. This design meets the stringent requirement of dissipating less than 200 mW per channel.

The ASIC is being designed by the EPFL/AQUA (CH) in 110 nm LFoundry and a prototype version of the ASIC featuring 8 channels will be submitted during the summer of 2023. It will be hosted on a high-speed printed circuit board designed by INFN/Padova (IT). A first prototype will be available by the end of the year, however equipped with commercial FADCs for the proof of concept.

2.3 Readout Architecture

A simplified view of the camera architecture is shown in Fig. 2.

Each channel composing a single pixel is connected to the pre-amplifying ASIC. A single output per pixel is fed to the Fast ADC ASIC that digitises continuously the signals. The pixels are grouped in clusters of 48 which amounts to a data rate of 576 Gb/s. These data, together

with the one of the neighbouring clusters are fed continuously to the so-called Level 1 (L1) trigger board developed by CIEMAT (ES). This board plays the fundamental role to collect and buffer the data until a positive trigger decision is taken. The waveforms are stored in ring buffers of 4 μs depth, which provides the latency necessary to await for a trigger signal coming from a neighbour telescope. Each L1 board also features a first level trigger that relies on the digital sum of the cluster pixel signals and its direct neighbours. When the first level trigger condition is met in at least one L1 board across the camera, the data from all L1 boards are funneled to the central trigger processing (CTP) board. At this stage, the requirement is that the L1 board can ship events and that the CTP can receive and process events at a rate of the order of 300 to 500 kHz.

The CTP board, being developed by Universidad Complutense de Madrid (ES), receives the data from all L1 boards of the camera and combines them to take a higher-level trigger decision. At this stage, the data input rate together with the FPGA processing capabilities, will allow the implementation of real-time deep-learning inference. Some preliminary work based on anomaly detection and convolutional neural networks has started but requires more development to ensure robustness of the outcome regardless of the NSB level. The goal of these new algorithms will be to more efficiently discriminate between NSB-induced and extensive air shower events as well as a lower sensitivity to fast NSB variation or bright objects such as stars in the camera field of view.

The CTP will also be able to generate a trigger signal (so-called pedestal trigger) or receive trigger signals from external sources (e.g. neighbouring telescope or calibration light source).

Eventually, the rate at which events are sent to the data acquisition hardware will range from 30 to 50 kHz, i.e., a factor of 10 smaller compared to the L1 trigger output rate. The event will not only contain the waveform of each camera pixel, but also include the output of the artificial intelligence network running on the CTP. This information will be fed to a software stereo trigger running in real-time at the data acquisition level. With the data of the two or more telescopes that will have triggers, a better trigger decision will be taken, decreasing by at least a factor of two the final event rate. Additionally, the algorithms will discriminate the data according to the following classes: gamma/electron, hadron and muon. This will, among other benefits, allow to tag muons in real time and ease the task of the real-time analysis. Additionally, the ability to tag hadronic events, before even writing them to disk, can be used to achieve the necessary data volume reduction helping to keep the storage cost within the CTAO cost book.

The data acquisition hardware will either be FPGA or GPU-based depending on the final data rate and the required processing capabilities.

Except for the front-end board (inside the camera) and data acquisition hardware (inside the on-site computer infrastructure), the location of each board is deliberately not indicated in Fig. 2 as still under evaluation. The criteria which are under consideration for this choice are the signal integrity, the power density and the total camera weight.

3. Conclusions

The design choices for the next generation of SiPM Cherenkov cameras for the LST are well advanced and have allowed to significantly ramp up the effort of the different institutes involved. In the course of the coming months, most of the hardware required for the proof-of-concept of the proposed architecture will be purchased and the development of the trigger algorithm, as well

as the different firmware required for their implementation, will be developed. The realisation of a complete camera slice, from a central trigger cluster and its neighbouring modules to the data acquisition hardware, is expected to be assembled by 2026 which will prove the feasibility and performance of the proposed architecture. The fully digital architecture will offer the upgradability required to maintain the highest level of performance for the future LST cameras. The stereo analysis of the simulated data is already ongoing both with a classical approach [13] and with novel analysis methods based on deep-learning [9].

4. Acknowledgment

We gratefully acknowledge financial support from the agencies and organisations listed under this link https://www.lst1.iac.es/acknowledgements.html

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