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A new front end electronics for the detection of the optical Cherenkov signals by Extensive Air Showers directly observed from sub-orbital and orbital altitudes

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We present in the following a new type of front-end electronics which has been developed for the detection of the optical Cherenkov signals by Extensive Air Showers directly observed from sub-orbital and orbital altitudes. It adopts a new generation of low-power consuming 64-channel Application-Specific Integrated Circuit (ASIC). The ASIC is implemented in a commercial 65 nm CMOS technology to readout an 8×8 matrix of SiPMs. The event is recorded in an array of 256 cells, each one equipped with an analog memory, a 12-bits Wilkinson Analog-to-Digital Converter (ADC) and latches running at a sampling rate of 200 MS/s. The converted data are sent off-chip to an FPGA which controls the readout operations of the ASIC channels and implements the trigger logic. The goal is to employ it on experiments either on balloon platforms or space-based which are devoted to Ultra-High Energy Cosmic Ray and neutrino astronomy from space through the detection of atmospheric Cherenkov light. We discuss in the following its suitability for EUSO-SPB2-like missions on board stratospheric balloons and for the Terzina project, part of the NUSES space mission.

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1. Introduction

The Cherenkov signal from an Extensive Air Shower (EAS) produced by an Ultra-High Energy Cosmic Ray (UHECR) or UHE neutrino seen from Low Earth Orbit (LEO) such as ~500 km height or sub-orbital height such as ~30-40 km is expected to last tens of ns, according to simulations, depending on the off-axis angle between the EAS direction and the telescope axis [1]. For this reason, the Front End Electronics (FEE) should have a time resolution in the order of 10 ns or less. Moreover, the possibility of recording the signal waveform would allow a more precise distinction of signals originating from an EAS compared to other signals in the detector such as those due to direct cosmic ray hits. Based on these scientific requirements, the INFN Torino, since August 2020, is developing a new type of Application-Specific Integrated Circuits (ASIC) which is expected to meet these constraints. The design is inspired by present and future projects in the field of UHECR and UHE neutrino astronomy such as EUSO-SPB2 [2] on board stratospheric balloon platform or Terzina [3] and POEMMA [4] space-based missions. The concept of the circuit is summarized in [5] and its evolutions in [6]. We describe in the following its suitability in the context of the NUSES and POEMMA-Balloon-Radio missions.

NUSES is a space mission for two innovative detectors dedicated to the study of cosmic radiation and the Sun-Earth environment [7]. The first is named Terzina [3, 8] and it is devoted to UHECRs beyond 100 PeV, while the second is named Ziré [9] and it is devoted to cosmic ray science below 250 MeV. The NUSES mission is planned to operate for about three years and the satellite, with the two payloads, will orbit at 550 km altitude at the beginning of life and at about 525 km at the end of life. The orbit inclination will be 97.6° with LTAN 18:00:00. Terzina is a satellite-based detector designed for Cherenkov light detection from EAS induced by UHECRs in the Earth's atmosphere at energies above a few hundreds PeV [1]. At the same time Terzina will point below the Earth's limb to monitor the atmospheric emissions as well as those from ground to characterize the light intensity and demonstrate the principle of observation of Earth-skimming UHE neutrinos [10]. The Terzina payload is composed by the following elements: the optical head unit, which is a near-UV-optical telescope, the focal plane assembly (FPA), the thermal control system, and the external harness and electronic units. The optical system of the telescope is based on a dual mirror configuration which has been chosen to maximize the focal length in the available space which is an envelope in the shape of a cut-cone with a 394 mm diameter and a 350 mm length. The resulting focal length is about 925 mm. The telescope is inclined 67.5° with respect to the nadir, having an optical axis pointing towards the Earth's limb (see [8] for more details). The FPA is conceived to detect photons from below and above the limb. It has a rectangular shape with a $2:5$ aspect ratio. It is composed of 10 SiPM arrays of 8×8 pixels each forming 2 rows of 5 arrays each. The sensors are FBK SiPMs based on NUV-HD-LowCT SiPMs technology [11]. The telescope has a field-of-view of 7.2° horizontally and 2.5°, as each pixel sees 0.18°. It can observe a vast volume of the atmosphere with a cross-section of 140×360 km^2.

The POEMMA-Balloon-Radio mission is still in a conceptual study but it will be largely inspired by the EUSO-SPB2 [2] mission which flew on board a NASA Super Pressure Balloon launched on May 13^{th} 2023 from Wanaka New Zealand. EUSO-SPB2 payload consisted of a Fluorescence Telescope with a Multi-Anode PhotoMultiplier Tube (MAPMT) camera pointed towards the nadir to record fluorescence light from UHECR EAS with energies above 1 EeV, and

a Cherenkov telescope (CTel) with a SiPM focal surface for observing Cherenkov emission of CR EAS with energies above 1 PeV with an above-the-limb geometry and of PeV-scale EAS initiated by neutrino-sourced tau decay. The CTel instrument is a 1m diameter modified Schmidt telescope with a bifocal alignment of the 4 mirror segments meaning light is focused in two distinct spots on the camera instead of one, helping to distinguish between direct cosmic ray hits (only one spot) and light from outside the telescope (2 spots), thereby reducing the background. The core of the Cherenkov telescope is a 512 Silicon PhotoMultiplier (SiPM: S14521-6050AN-04 from Hamamatsu) pixel camera with an integration time of 10 ns and a readout depth of 512 frames centered around the trigger, allowing to target very fast and bright signals, like the Cherenkov emission from EASs to achieve the goals outlined earlier. The FoV of the instrument is 6.4° in zenith and 12.8° in azimuth and can be pointed during the flight from horizontal to 10° below the Earth's limb depending on the targeted science. A more in-depth discussion of the instrument can be found in [12].

2. The Front end Electronics

The main characteristics of this ASIC concept are as follows. The 64-channel ASIC is implemented in a 65-nm CMOS technology for the readout of SiPMs. Each channel embeds a front-end amplifier which employs the common gate topology followed by 256 memory cells with a sampling frequency of 200 MHz. A single cell includes a storage capacitor, a single-slope Analog-to-Digital Converter (ADC) with programmable resolution between 7 and 12 bits and a digital control logic. This architecture allows the ASIC to digitize all the samples in parallel reducing the conversion deadtime. Moreover, the digitization is carried out only if a trigger signal validates the time window thus saving power. The memory cell arrays can be divided in shorter slots of 32, 64 or 256 cells each which can work in parallel. The use of a segmented analog memory results in the derandomization of the Poisson distributed data further reducing the dead time. The target power consumption is 5 mW/ch (Fig. 1 left).

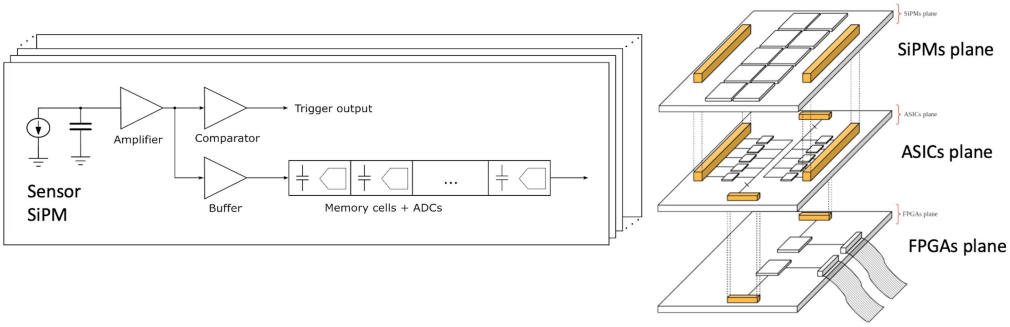

Figure 1: Left: Concept of the ASIC channel block diagram. Right: The camera architecture with SiPM, ASIC and FPGA planes.

The overall architecture of the camera is shown on the right side of Fig. 1. The structure is organized in three planes: one PCB for the sensors, one for the ASICs and the third one with FPGAs to read out the ASICs and generate a trigger signal. Concerning the readout and trigger mechanisms, the ASIC incorporates the capability of programming two thresholds per channel, referred to as the low (S_0) and high thresholds (S_1). Upon surpassing S_0, a programmable counter

begins counting for a brief period of clock cycles, approximately 20 ns, in order to verify whether the signal originates from an event or from electronic noise and fluctuations. If, within this time frame, S_1 is also exceeded, only S_1 is transmitted to the FPGA; otherwise, S_0 is transmitted. A request for reading is then dispatched to the FPGA, which should provide a consent to read the data in a time window $\Delta t_c = WAIT\_CNT * T_{clk}$, which should not exceed 16 clock cycles ($WAIT\_CNT$) of T_{clk} = 5 ns each, equivalent to 80 ns (the precise limit depends on the number of memory blocks specified in the ASIC's configuration). After this period, the FPGA evaluates and either accepts or rejects the hitmap. In the case of acceptance, the ASIC can proceed to digitize and transmit the data; otherwise, it reverts back to the sampling stage.

A single hitmap consists of 112 bits, with 98 bits representing the actual hitmap data and an additional 14 bits allocated for overhead. The total time required to transfer the hitmap from the ASIC to the FPGA is estimated to be 140 ns. Once the hitmap is successfully transferred to the FPGA, it proceeds with the recognition of specific hitmap topologies, that typically takes ~30 ns. Three distinct scenarios can arise:

1. *Event Recognition*: The FPGA accepts the data when the following conditions are met:
   - S_1 is exceeded in a single pixel or, alternatively, in two adjacent pixels.
   - S_0 is exceeded in two adjacent pixels or, alternatively, in three adjacent pixels or, alternatively, in four adjacent pixels.
2. *Data Rejection*: The FPGA rejects the data within the designated time window Δt_c if there are insufficient adjacent pixels above the threshold in the hitmap. In the case where a single pixel exceeds the threshold at the border of the tile, the FPGA proceeds to check the adjacent ASICs to search for events across multiple ASICs using the pattern recognition algorithm previously described, which may result in the acceptance or rejection of the event.
3. *No Response*: If the FPGA fails to respond within the time window Δt_c, the event is rejected, and the discriminators are monitored once again for subsequent events.

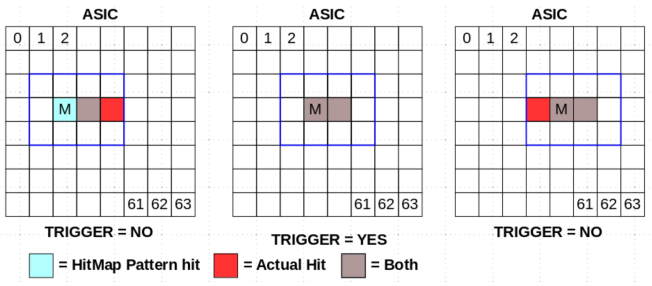

Figure 2: Pattern seeking algorithm: each pixel is considered as main (M) and the pattern fingerprint is checked. This procedure is done in parallel for every pixel and every pattern case.

Once an event is accepted (as described in case 1 above), it undergoes centering for digitization at time t_S, which corresponds to the moment when the threshold is exceeded. As the ASIC is highly flexible and it is possible to store 32, 64, till 256 memory cells and the number of bits can vary between 8 and 12 we will consider in the following only one case which is expected to be the most

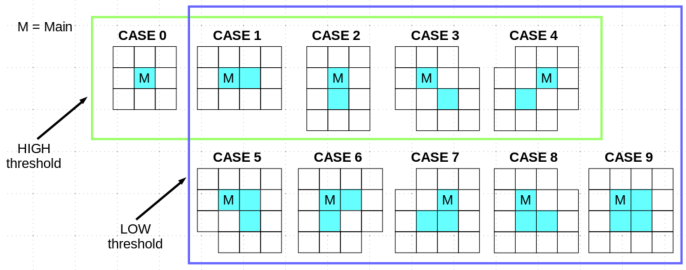

Figure 3: Hitmap validator pattern case: different pattern searched by FPGA to accept or reject data.

suitable one for the present application which is: 8 independent blocks of 32 memory cells each, equivalent to 160 ns time window for waveform digitization and storage, and 12 bit resolution in signal amplitude. Digitization is accomplished by sampling the signal at 32 time-points, spaced by T_{clk}, from $t_S - 80$ ns to $t_S + 80$ ns. Each channel (pixel) requires one memory block for storage. The maximum time required by the ASIC to digitize an event is upper-bounded by $2^{12}T_{clk}$, equivalent to 20.5 μs. It is important to note that while one block of cells is engaged in the digitization process, the remaining 7 blocks are available to register new hitmaps and repeat the processes of sampling and digitization. These operations can proceed in parallel across the 8 memory blocks of the pixels. However, if all memory blocks are occupied (8 blocks in use) simultaneously, only the hitmap can be sent to FPGA, while the ASIC will not be able to store new data until all the data in memory has been processed and transferred to the FPGA.

The digitized signal within a single pixel is encoded using a number of bits, specifically $12 \times 32 + \text{header} + \text{padding}$, resulting in a total of 434 bits. When considering an event in a single ASIC, it is encoded using $64 \times 434 = 27776$ bits. The time required for the ASIC to transfer an event to the FPGA is calculated multiplying the number of bits by 1.25 ns (as the FEE adopts a 400 MHz serializer in DDR), resulting in 34.7 μs. Taking into account the ASIC's capability to handle 8 parallel chains and assuming that one FPGA can concurrently manage 8 chains per ASIC for a total of 5 ASICS, the ASIC experiences deadtime only when the memory blocks reach maximum capacity, meaning all 8 blocks are occupied simultaneously. However, this deadtime is always shorter than the time required to transfer an event from the ASIC to the FPGA (34.7 μs).

3. Simulation of the detector and FEE response

A simulation code has been developed to examine the response of the detector waveform. For this study the Terzina case has been assumed. This simulation chain serves as an initial step to study the geometry and evaluate performance. To assess the sensitivity and performance concerning the expected UHECR signal, a dedicated generator has been integrated into the simulation code. Specifically, the Emission for Extensive Air Showers Cherenkov Simulation (EASCherSim) [1, 10] is employed as the physics event generator. EASCherSim provides essential parameters such as the average photon density and spectral composition, photon angle in relation to the shower axis, and its timing. The simulation code is based on the knowledge of the sensor's single photoelectron signal, which is shaped by the amplifier, as well as the sensor's noise rate and night glow background (NGB). These simulations offer valuable insights into comprehending the necessary parameters of

the sensors. Additionally, they aid in establishing the trigger logic and assessing the effectiveness of the hitmap pattern recognition algorithm that will be implemented on the FPGA. In the simulation studies the following typical characteristics for an FBK 35 μm cell-size sensor have been assumed: dark count rate (DCR) ~100 kHz/mm^2, afterpulsing (AP) ~5%, optical crosstalk (CT) ~5–20%, and photodetection efficiency at peak (PDE) ~50–60% in the blue region of the light spectrum.

The SiPM's response to the night sky background light is evaluated employing a simple toy model as proposed in [13]. The model can be described as follows: each simulated waveform is discretized into samples with a width (Δt) of 1 ns. For every sample, the photon generation process begins by randomly generating photons following a Poisson distribution with a mean value of $F_{ph}(i) \cdot \Delta t$, corresponding to the photon rate associated with a given wavelength distribution, F_{ph}. Each generated photon is individually processed to determine whether it is detected or not, based on its wavelength and PDE. The SiPM uncorrelated noise, influenced by the DCR, is added to the system. Additionally, the total number of photons is randomly increased by accounting for crosstalk and afterpulses, resulting in the determination of the total number of avalanches for sample i, $N_{av}(i)$, each with its own corresponding generation time. The $N_{av}(i)$ value is then converted into a SiPM current, I_{SiPM}, using the formula:

$$I_{SiPM} = F_{av} \cdot \frac{C_{\mu cell} \cdot \Delta V(i)}{e} = \frac{N_{av}(i)}{\Delta t_i} \cdot G(\Delta V(i)),$$

where F_{av} is the avalanche rate, $C_{\mu cell}$ the microcell capacitance which determines the SiPM gain $G(\Delta V(i))$. At this stage, the gain is subject to random smearing with a Gaussian distribution characterized by a standard deviation σ_G, representing the gain fluctuation of the SiPM across different microcells. Using I_{SiPM}, voltage drop is calculated, and both variables are used to estimate the impact on the overvoltage in the subsequent sample, and to derive the values of all parameters for sample i + 1. When reaching the last sample, $i = N - 1$, the experimental waveform is generated as the sum of all the previously generated avalanches, $N_{av}(i)$, convoluted with the template of the normalized SiPM pulse and shifted by the initial electronic baseline. Furthermore, each waveform value is randomly smeared by a Gaussian distribution with a standard deviation σ_e, representing the electronic noise of the system under consideration. Waveforms were simulated for a time frame of 10^7 ns under various NGB+DCR conditions. Counting the numbers of peaks below a given threshold divided by the simulated time frame, trigger rates can be estimated.

In order to simulate a Cherenkov event, the process begins with a shower generated by EASCherSim. A random pixel is selected as the target, and the incoming photons are distributed across adjacent pixels, taking into consideration the Point Spread Function (PSF). This results in a map of the affected pixels and the corresponding number of photons. During the simulation of the entire camera plane, the code determines whether a pixel has been hit by a Cherenkov event. If a pixel is found to be affected, the model retrieves the number of photons associated with that pixel from the map and incorporates them into the simulation chain. This allows for a representation of the camera's response to Cherenkov events within the simulation.

The code also incorporates the trigger logic as described previously. When the high threshold is surpassed by at least one channel, a binary hitmap is stored. In the case of the low level threshold trigger, a binary hitmap of the corresponding ASIC(s) is generated when at least two pixels cross the low threshold within a single ASIC or along the edges of two neighboring ASICs. The generated

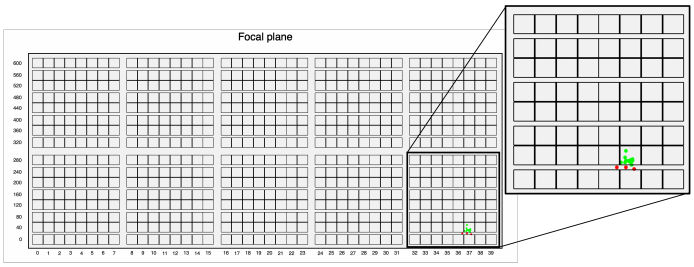

Figure 4: Visualization of a simulated shower projected onto the focal plane. Detected photons are depicted as green dots, while discarded photons are represented by red dots.

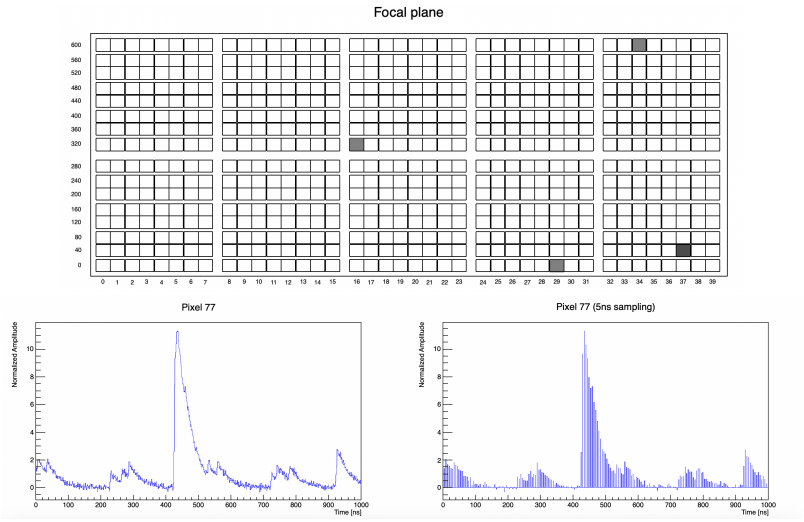

Figure 5: Example of an event triggering a high threshold S1 trigger. The top image shows the binary hitmap of the entire focal plane corresponding to the event. The bottom section displays the simulated waveform of the triggering event, along with the waveform sampled every 5 ns.

hitmap is then analyzed to identify the presence of at least two adjacent channels that exceed their respective thresholds, forming a cluster. If a cluster is detected, the hitmap is saved. This process yields a substantial data sample that has been used to test and enhance the trigger logic as well as the pattern recognition algorithm, which will be implemented in the FPGA.

4. Conclusions

A new type of FEE for the detection of the optical Cherenkov signals by EAS directly observed from sub-orbital and orbital altitudes has been described. It is based on a new type of ASIC which is specifically developed for space applications with low power consumption (<5 mW/channel) and sufficiently radiation hard. The ASIC's 200 MHz clock frequency enables a precise waveform sampling to clearly recognize an EAS Cherenkov signal from other types of sources such as direct cosmic ray hits, noise spikes or atmospheric events. The developed trigger logic is capable of reducing the fake event rates and the data overhead in order to downlink all the events of interest. The hitmaps also allow the possibility of triggering on signals generated by a bi-focal system. This is considered to be another key way to uniquely recognize an EAS event.

5. Acknowledgments

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