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SBND Hardware Trigger System

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The SBND experiment is a liquid argon time projection chamber (LArTPC), which serves as the near detector to the Short Baseline Neutrino (SBN) program at Fermilab. With only 110 m between the detector volume and the beam target, SBND will record over a million of neutrino interactions per year, more than any LAr experiment to date. Furthermore, the detector is located on the surface and exposed to cosmic rays. As a result, a sophisticated and reliable trigger system is needed to ensure high efficiency of neutrino data while maintaining data rates which are manageable in downstream analysis. This proceeding will detail how the SBND trigger system achieves both of these goals.

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1. Introduction

The SBND experiment is one of three liquid argon time projection chambers (LArTPCs) that comprise the Short Baseline Neutrino (SBN) program at Fermilab [1]. The three detectors are located along the Booster Neutrino Beam (BNB) delivering a beam of predominantly ν_μ (93.6%) by impacting 8 GeV protons on a beryllium target. The primary goal of the SBN program is to perform precision measurements of neutrino properties and give a conclusive result on the eV-scale sterile neutrino hypothesis.

Located only 110 m away from the BNB target, SBND will serve as the near detector for the SBN program, measuring the composition of the beam to be compared to the oscillated flux at the far detector. Importantly, its proximity to the target will yield great statistical precision for measurements of ν-Ar interactions and searches for Beyond the Standard Model (BSM) physics.

The SBND detector has its active volume divided into two drift volumes by a central cathode plane, which will operate at high voltage (-100 kV). The anode plane walls on either side of the cathode will be kept on ground, resulting in 500 V/cm electric field allowing ionisation electrons from charged particle passages through liquid argon to drift towards the anodes and be read out. In addition to the TPC ionisation signals, SBND will record the scintillation light produced by charged particles in liquid argon using a photon detection system (PDS). The PDS consists primarily of 120 8” Hamamatsu R5912 photomultiplier tubes (PMTs) installed behind the anode wire planes. Furthermore, 192 novel photon detectors, X-ARAPUCAs, will be employed. Finally, a cosmic ray tagger detector system (CRT), composed of panels of scintillator strips, will surround the outside of the cryostat and be used for cosmic background tagging.

2. Hardware Trigger in SBND

The SBND hardware trigger system is responsible for ensuring high efficiency of recording neutrino interactions while limiting the total data rate to 1 Hz. The BNB spill rate is 5 Hz and a neutrino interaction is expected approximately every 20 spills. Furthermore, SBND strives to search for beam-related BSM physics for which low trigger threshold is necessary. These interactions have to be selected from kHz of cosmics interacting in SBND due to its location on surface.

The trigger in SBND is based on the PDS as the time of flight of the scintillation photons is significantly faster (order of ns) compared to the drift times of the ionisation electrons in the TPC (order of ms). The electronics boards responsible for making the trigger decision are the Penn/Photon Trigger Board (PTB) and the Master Trigger Card Analog (MTC/A), shown in Figure 1. Together these boards allow for triggering on light activity across the detector (localised or spread out) paired with programmable logic (BNB coincidence, pre-scaled spills, CRT triggers etc.).

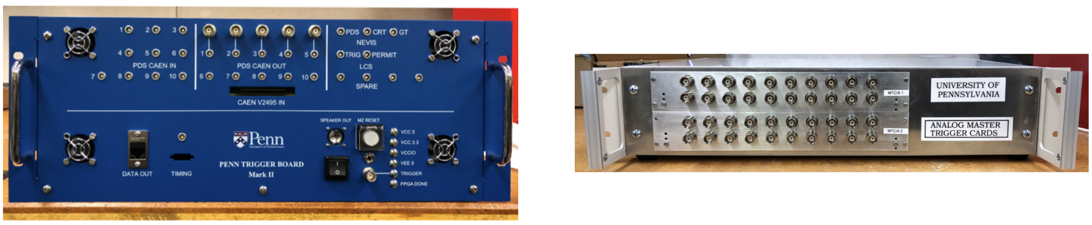

Figure 1: Photos of the PTB (left) and the MTC/A (right).

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The primary trigger for neutrino interactions will be a scintillation light flash detected by the PMTs in coincidence with a beam spill. The PMT signals are digitised by CAEN V1730 boards (16 PMT channels per board), which are able to provide digital trigger pulses if a predetermined number of PMT pairs crosses their threshold. This way, however, it is only possible to trigger on the number of CAEN boards over threshold, rather than total number of PMT channels. The MTC/A, which was repurposed from the SNO experiment, facilitates a trigger on the number of individual PMTs over threshold. The MTC/A takes the signals from the CAEN boards which are proportional to the number of channels over threshold and performs an analog sum across all of the boards, resulting in a single detector-wide sum. Finally, this analog sum is compared to 3 programmable thresholds and a logic pulse is sent out to the PTB if its magnitude is greater than the set threshold. Finally, the PTB is responsible for combining these signals with any other signals and programmed FPGA logic and issue a trigger to prompt detector data read out. Figure 2 shows the signals involved in the described trigger path. The trigger is issued with latency of $O(100\text{ ns})$, which is insignificant compared to the readout window of the TPC.

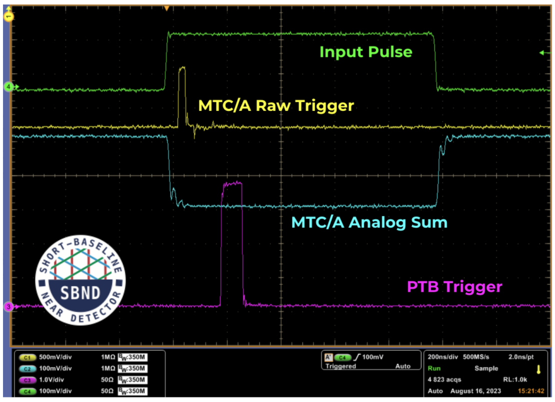

Figure 2: A scope shot from PTB and MTC/A testing of the trigger path. The fake PDS input pulse to the MTC/A (green) produces an inverted analog sum (turquoise) and upon crossing a programmed threshold, the MTC/A emits a 20 ns logic pulse (yellow) to the PTB, which emits a readout trigger (purple).

3. Penn Trigger Board

The PTB in SBND takes inputs from the PDS, the CRT, and beam instrumentation, which indicate the arrival of a BNB spill. These input signals are used to form a trigger decision using programmable FPGA logic in the PTB firmware and distribute it back to the detector subsystems (PDS, TPC). The photo of the PTB enclosure is shown in Figure 3.

The PTB is a highly flexible, programmable and configurable trigger board and its versions are currently also used in the ProtoDUNE and EOS experiments [2, 3]. The board houses a commercial MicroZed$^{\text{TM}}$ board containing a Zynq$^{®}$-7Z020 System-On-a-Chip (SoC), which provides user-programmable FPGA logic and a processing system with direct access to the FPGA. The hardware trigger logic is defined through experiment-specific firmware on the FPGA with the option for run-time configuration.

In order to interface with different readout electronics and detector subsystems that use a variety of signal logic standards, the PTB contains a range of translator circuits, which are responsible for converting the input signal to the same flavour (3.3V LVCMOS) before passing them to the

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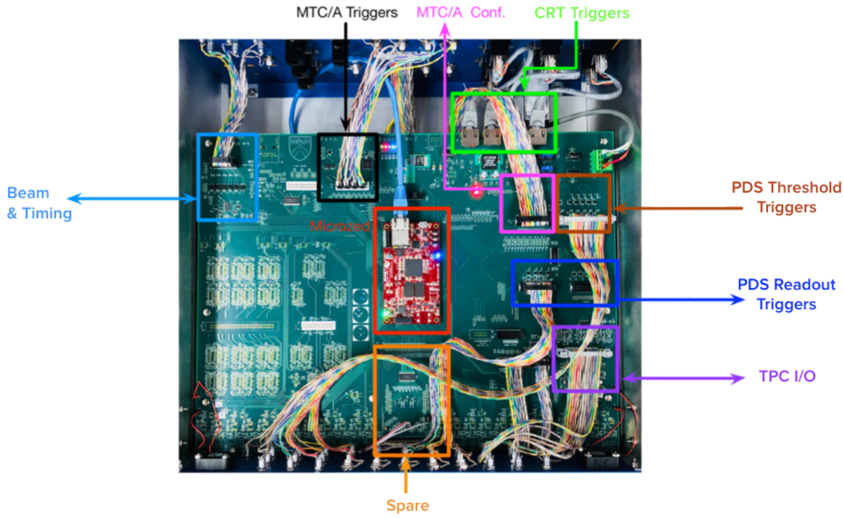

Figure 3: A photo of the inside of the SBND PTB enclosure, showing logic signal conversion circuitry and MicroZed in the middle. The Input/Output regions for the different SBND subsystems are labeled.

MicroZed^{TM} as well as converting the outputs to flavours required by the given systems (NIM, TTL, ECL, LVCMOS). Altogether the PTB has $\sim$ 100 input and outputs.

The PTB firmware architecture provides flexibility in hardware triggering; the inputs from individual subsystems are first combined into low level triggers (LLTs), which are in turn combined into high level triggers (HLTs) across all subsystems. The logical combination (AND, OR, NOT, >) of the signals within each is LLT and HLT is configurable at run-time. Furthermore, the firmware allows for configurable masking, delays, and shaping for all inputs and outputs. As a result, a number of sophisticated trigger options is available, including coincidences (eg. light and beam), vetoes, off-beam triggers for background studies, crossing muon trigger for commissioning, and multiple short PDS trigger windows per TPC readout.

4. Conclusions

SBND aims to achieve world-leading measurements of neutrino interaction properties and searches for BSM physics. Efficient and configurable hardware trigger is employed to optimise detector readout for maximal physics sensitivity given data size restrictions. The SBND detector, including the trigger system, is currently being commissioned and first liquid argon data is expected in early 2024.

References

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