The new ODMB for the Phase II upgrade of the CMS endcap muon system

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The proton-proton collision rate at the High Luminosity LHC will impose significant challenges on the data acquisition system used to read out the CMS Cathode-Strip Chamber (CSC) Muon detectors. These chambers are located in the endcap regions of the CMS detector, and those closest to the beam line encounter a particularly high particle flux. To address these issues, a major upgrade of the electronics used in the CSC system has been undertaken. A key part of this upgrade is the development of new Optical Data-acquistion MotherBoards (ODMBs), which collect both the anode-wire and cathode-strip data. The ODMBs feature powerful Xilinx Field Programmable Gate arrays and include interfaces with high-speed optical transceivers operating at up to 12.5 Gb/s. The requirements, design, implementation, and testing of the ODMBs will be discussed, and the performance of prototype boards will be presented.

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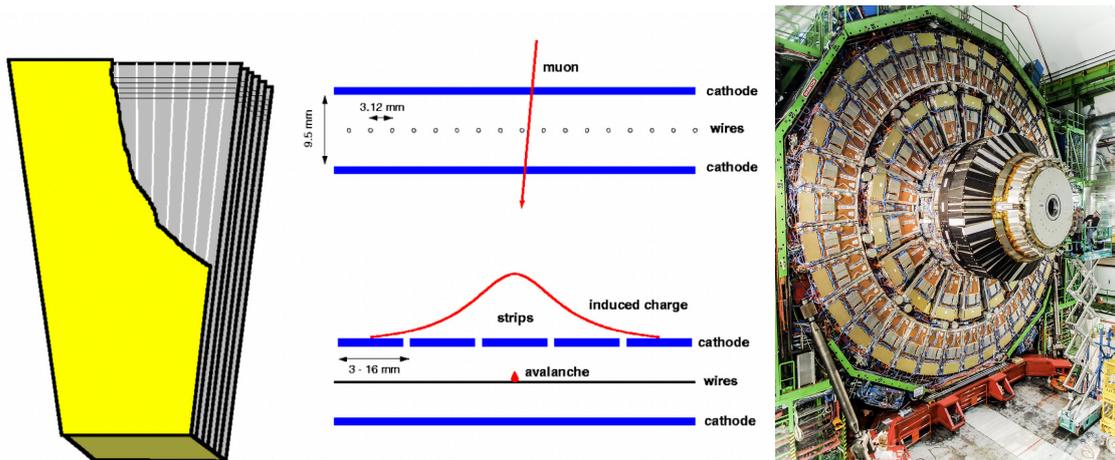
Figure 1: Left: Layout of a CSC chamber, 7 trapezoidal panels form 6 gas gaps. Only a few wires (lines running from left to right) and strips (gray band running from top to bottom) on the top right corner are shown for illustration. Middle: Working principle of CSCs in a single gas gap. Right: Pictures of CSCs from the station closest to CMS interaction point.

The CSCs are multi-wire proportional chambers with a finely segmented cathode strip readout. The strips run radially in order to measure the muon position in the bending plane (the plane perpendicular to the colliding beams axis), while the anode wires run azimuthally and provide a coarse measurement in the radial direction, *R*. A precise measurement of the muon coordinate as it traverses the chamber in the azimuthal direction (ϕ in the CMS coordinate system) is obtained from charges induced on cathode strips. Each CSC module consists of six gas layers, each layer having a plane of radial cathode strips and a plane of anode wires running perpendicular to the chamber's central radial strip. Figure 1 illustrates the operation of the cathode strip chambers and shows some of the CSC chambers during installation in the CMS detector. The gas mixture is 40% Ar, 50% CO_2, 10% CF_4. The primary design consideration for the CSC detectors is the ability to provide good spatial and temporal resolution for the triggering, identification and reconstruction of a muon.

The electronics readout system of all CSC chambers until LHC Run 2 is summarized briefly below, also shown in Figure 2. On each CSC chamber, the anode and cathode signals are sampled and digitized by Anode front-end board (AFEB)/Anode Local Charged Track(ALCT) and Cathode front-end board (CFEB) respectively. For CSCs closest to the interaction point (ME1/1 chambers), all the CFEBs were replaced by the Digital CFEB (DCFEB) during Long shutdown 1 (LS1). During the LS2, the DCFEBs serving the ME1/1 chambers were replaced by the DCFEB_v2 with more radiation hard optical transceivers and allowing the PROMless programming of its FPGA in case its EEPROM failed to work due to high radiation does. The CFEBs used for ME234/1 chambers were replaced by a combination of DCFEB and DCFEB_v2 in the same peirod during the LS2. The Trigger mother board (TMB) for each chamber , or Optical TMB (OTMB) for ME1/1, builds trigger primitives for CMS level 1 trigger decision. Each chamber is also equipped with one Data aquisition mother board (DMB), or Optical DMB (ODMB), it is responsible for slow control, distributing trigger signals, LV control/monitoring and to take data from ALCT, DCFEB, OTMB to build data packet and send to the DDU board at a rate up to 1.6 Gb/s. DDU is short for Detector data unit, it collects data from 15 (O)DMBs and sends information to CMS global DAQ
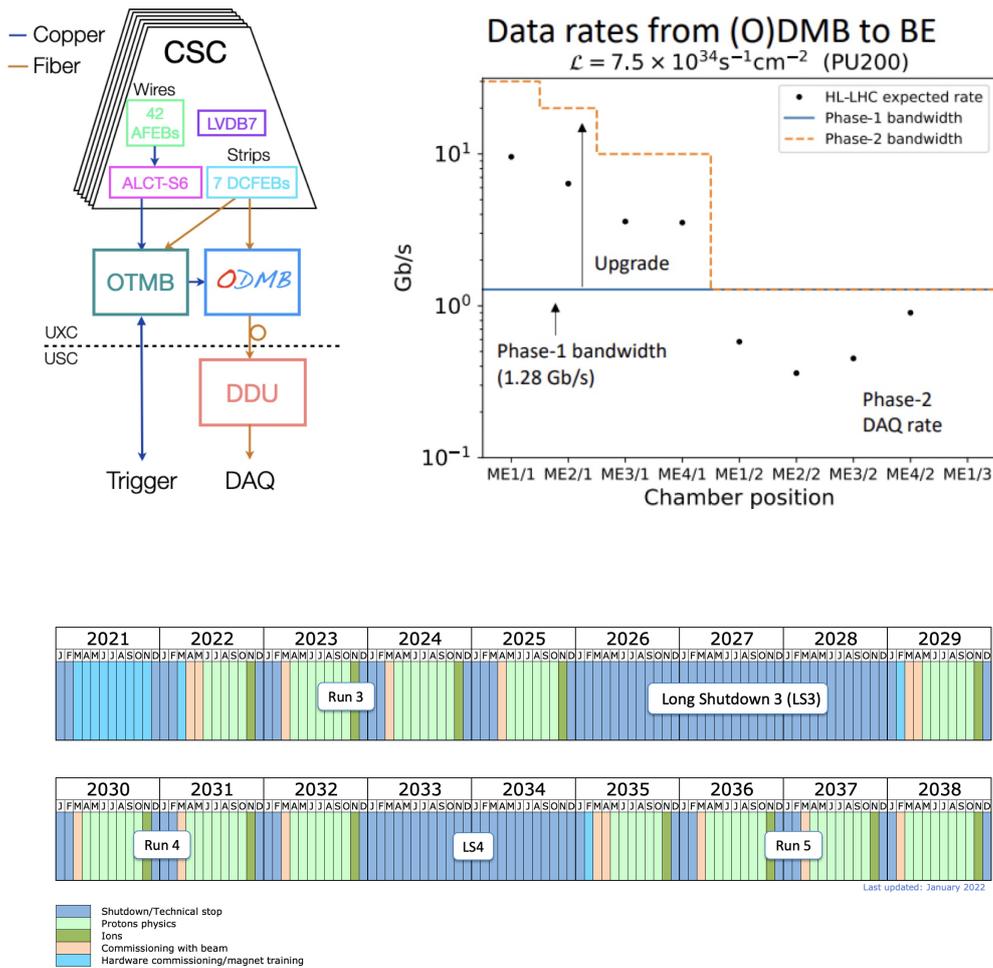
Figure 2: (Top left) The schematics of CSC's electronics readout system. (Top right) expected data rate for different types of CSC chambers at HL-LHC condition, as well as current bandwidth of DMB and ODMB. (Bottom) HL-LHC operation schedule.

According to the current schedule (Figure 2, the high luminosity LHC (HL-LHC) will start operation on 2029 with about 7 times higher collision rate comparing to the past LHC Run 2. At HL-LHC condition, the upgraded DCFEBs can produce data for transmission to the ODMB at a rate up to 3.2 Gb/s and together with ALCT and OTMB can produce a total data rate up to 10 Gb/s to the ODMB, and for ME234/1 chambers, the expected data rate from DCFEB + ALCT + OTMB will be 3-5 Gb/s. These rates exceed current bandwidth of the DMB and ODMB (1.6Gb/s), as these chambers suffer from higher particle flux comparing to other CSCs in the system. New ODMB7 and ODMB5 have been designed to serve ME1/1 and ME234/1 for HL-LHC operation, ODMB7(5) will interact with 7(5) DCFEBs from the ME1/1(ME234/1) chambers, that's where the 7 and 5 in the names come from. ODMB7/5 utilize state-of-art Xilinx Kintex Ultrascale FPGA, each FPGA contains 16 GTH transceivers with 16Gb/s maximum data transferring speed. To allow for at least a factor of 3 safety margin, e.g. maximum bandwidth per board 3 times higher than expected data rate, ODMB7 and ODMB5 are equipped with 4 and 3/2 Firefly optical transceivers

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(up to 14 Gb/s rate per transceiver) for transmitting data to the next stage of CMS DAQ unit. The interfaces between the ODMB7/5 and other CSC electronics (DCFEB, OTMB, CCB, VME crate) are not changed with repect to the current ODMB. The maximum allowed data rate for ODMB7 (ODMB5) will be 50Gb/s and 25 or 37.5Gb/s (depending on the number of Firefly transceivers), which significantly exceed the expected data rate for ME1234/1 shown in Figure 2.
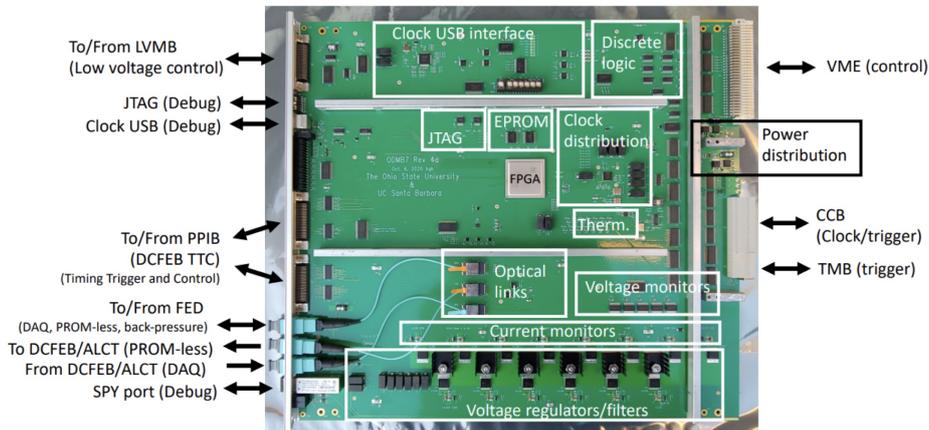
Figure 3: A picture of ODMB7 prototype.

As of 2022, 4 ODMB7 and ODMB5 prototypes have been fabricated, an example of ODMB7 prototype is shown in Figure 3. All interfaces (VME crate, other CSC electronics, SPI EPROM) for ODMB7/5 prototypes have been verified to be working in both UCSB and CERN with dedicated testing firmware and software. Figure 4 shows the a complete set up of CSC electronics system at UCSB lab used for testing the ODMB7/5 prototypes, and a similar arrangement with a real CSC chamber has been used at CERN testing site to verify all the functionalities of the new ODMB. Recently an ODMB7 prototype was used at CERN test stand to successfully take cosmic data with a real CSC chamber. Figure 5 shows the occupancy of the cathode data aquired by the new ODMB7 prototype during a cosmic data taking. The occupancy distribution matches that taken by a legacy ODMB board. Output from the logic analyzer is shown in Figure 6 with several features of the data annotated, all signals are as expected.

The upgraded optical data mother boards, ODMB7/5, which collect and transmit the full cathode and anode data output of the CSC chambers have has been discussed including the successful results of testing with CSC chambers. The new data motherboard can achieve a data throughput rate of 25-50 Gb/s which is substantially more than the expected HL-LHC data rate from the CSC chamber of 3-10 Gb/s and will allow fully efficient data taking with no data losses even at the highest luminosities.

References

[1] CMS Collaboration, The CMS experiment at the CERN LHC, JINST 3 (2008) S08004, doi:10.1088/1748-0221/3/08/S08004
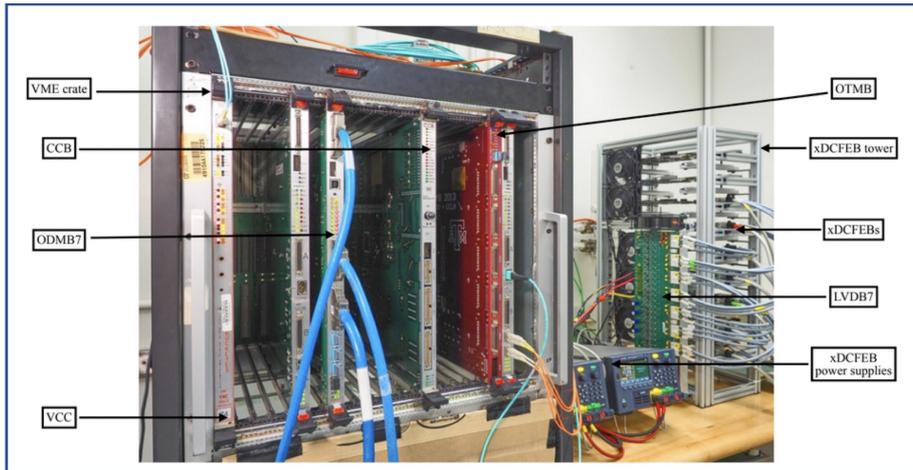
Figure 4: Full chain of CSC electronics at UCSB lab.
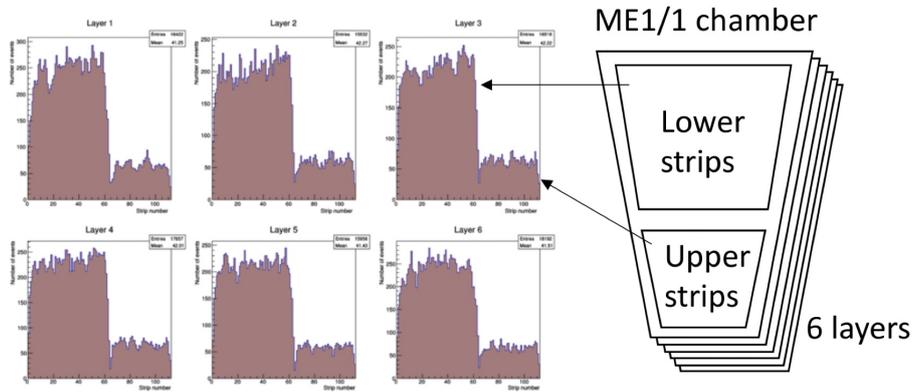
Figure 5: Cathode data distribution for ME1/1 chamber at CERN teststand, data was taken with a new ODMB7 prototype.
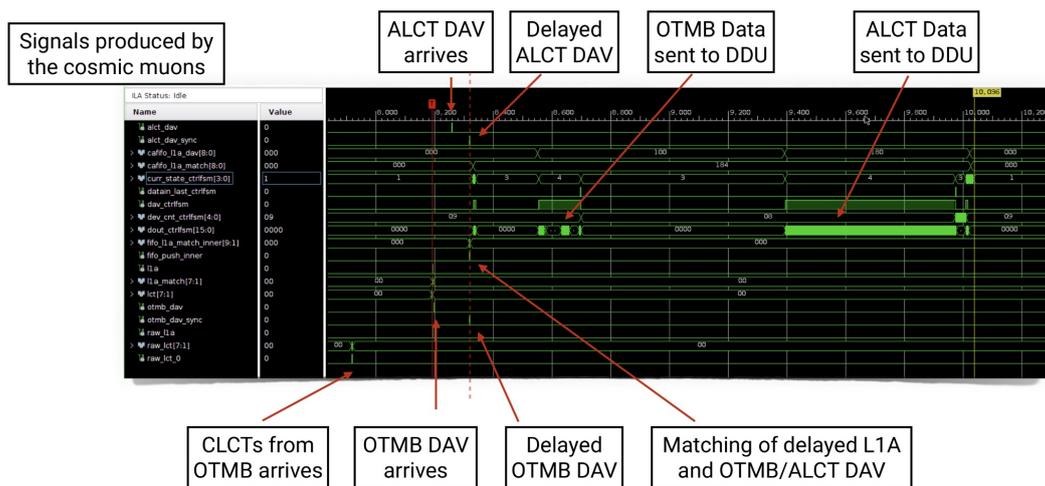
Figure 6: Examine key DAQ signals with a logic analyzer.