PROCEEDINGS OF SCIENCE

The Phase-2 Upgrade of the CMS Inner Tracker

Sergio Sánchez Cruz[a,*] **on behalf of the CMS Tracker Group**

[a] *University of Zurich, Switzerland*

E-mail: sergio.sanchez.cruz@cern.ch

The High Luminosity Large Hadron Collider (HL-LHC) at CERN is expected to collide protons at a center-of-mass energy of 14 TeV and reach the unprecedented peak instantaneous luminosity of $7 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$. This will allow the ATLAS and CMS experiments to each collect integrated luminosities of up to 4000 fb^{-1} during the project lifetime. To cope with this extreme scenario the CMS detector will be substantially upgraded before starting the HL-LHC, a plan known as the Phase-2 upgrade. The entire Inner Tracker (IT) detector will be replaced and the new detector will feature increased radiation hardness, higher granularity and capability to handle higher data rates. The detector is composed of pixel sensors with a pixel size of 2500 μm^2 and a new ASIC, designed in 65 nm CMOS technology, powered using a novel serial scheme. The system mechanics will be lightweight, based on carbon fiber, and will use a CO_2 cooling scheme. In this contribution, we describe the design of the IT system along with the latest results on prototype system testing.

41st International Conference on High Energy physics - ICHEP2022
6-13 July, 2022
Bologna, Italy

*Speaker

PoS(ICHEP2022)637

1. Introduction

The High Luminosity Large Hadron Collider (HL-LHC) at CERN is projected to deliver an integrated luminosity of up to 4000 fb^{-1} of proton-proton collisions over its 10 year lifetime. To do so, the delivered instantaneous luminosity will reach a peak of $7 \times 10^{34} cm^{-2} s^{-1}$ with up to 200 overlapping proton-proton collisions per 25 ns bunch crossing, also known as pileup. Due to these harsh conditions, the innermost part of the CMS detector, the pixel tracker, will need to survive a harsh radiation environment; a total ionizing dose of up to 1.5 Grad, and neutron-equivalent fluences of up to $2.6 \times 10^{16} n_{eq}\, cm^{-2}$. The current pixel tracker [1] cannot withstand these high radiation and occupancy conditions while maintaining a sufficiently high efficiency. In order to be able to deliver the same performance as the current pixel detector achieves under nominal LHC conditions, a new pixel detector has been designed to replace it.

The new Inner Tracker detector [2] will be composed of modules using pixelated sensors. The detector will be laid out in three different sections: the TBPX, composed of four barrel layers and covering the central region of the detector, the TFPX, composed of 16 concentric vertical disks, and the TEPX, composed of 8 disks. The upgraded detector will have an increased acceptance covering regions with $|\eta| < 4$ with at least four pixel layers. The size of the pixels has been reduced by a factor of 6 with respect to the current detector to $100 \times 25\, \mu m^2$ to keep the mean occupancy low and increase the detector spatial resolution.

Each module is composed of the pixel sensor matrix, the read-out chip to which it is bump-bonded, and a high-density interconnect (HDI), in which the powering and read-out connections are located.

2. Sensor design and performance

Pixel sensors are designed using n-in-p silicon, in contrast to n-in-n sensors used in the current detector, achieving a better radiation hardness due to their reduced thickness.

Two different topologies are considered in the design of this sensor. In so-called planar sensors, the electrodes are formed by an n^+ implant in the top surface of the sensor. In contrast, in 3D sensors, the electrodes are implanted as narrow columns penetrating the substrate. The advantage of 3D sensors is that they can achieve full depletion with a lower bias voltage and, since the free mean path of charge carriers is smaller than for planar sensors, they are less vulnerable to charge trapping and are therefore more radiation-hard. Their fabrication process, however, is more complicated than for planar sensors and, for this reason, their usage is only foreseen in the innermost layers of the detector where the fluence and therefore detector degradation are expected to be larger.

The performance of planar and 3D sensors is summarized in Fig. 1, which shows the hit efficiency as a function of bias voltage for sensors after different degrees of irradiation. Planar sensors were irradiated to fluences ranging from $0.8 \times 10^{16} n_{eq}\, cm^{-2}$ to $2.0 \times 10^{16} n_{eq}\, cm^{-2}$. The results show that an efficiency of 99% can be achieved with bias voltages of 600 V for sensors irradiated up to $1.2 \times 10^{16} n_{eq}\, cm^{-2}$. However, for sensors irradiated with a fluence larger than $2.0 \times 10^{16} n_{eq}\, cm^{-2}$, this efficiency is only achieved with bias voltages higher than 800 V. Thermal simulations show that in this regime the power consumption of the sensor increases significantly, resulting in a high risk of thermal runaway. In contrast, 3D sensors were irradiated up to a neutron-

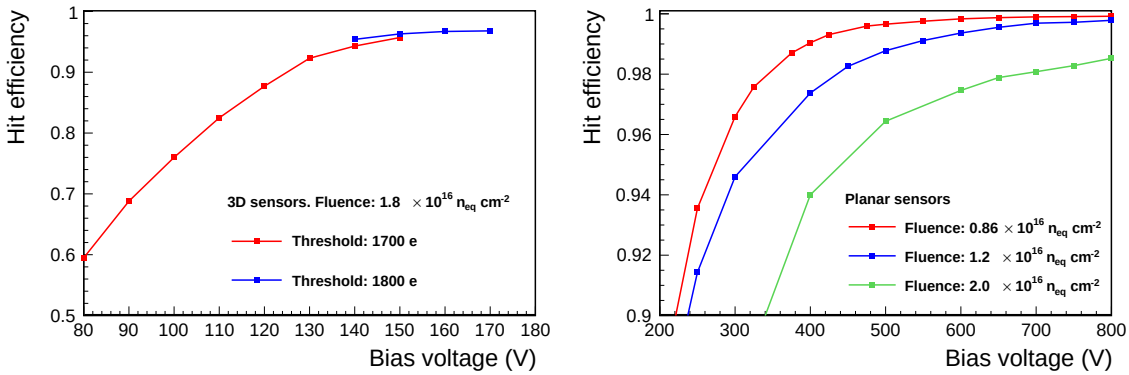

Figure 1: Hit efficiency of 3D (left) and planar (right) sensors as a function of the bias voltage applied to the sensor for different settings and irradiation scenarios.

equivalent fluence of 1.8×10^{16}n$_{\text{eq}}$ cm^{-2} and show a hit efficiency greater than 98% for bias voltages above 170 V. Under these conditions, the power consumption of the system is much reduced leaving a relatively large margin to operate the system in a safe thermal status.

3. Readout chip performance

Bump-bonded to the sensor, the readout chip is one of the key components of the Inner Tracker. The readout chip has been designed by the RD53 Collaboration [3] to withstand total ionization doses of 1 Grad and maximum rates of 3 GHz cm^{-2}, keeping the hit rate in the absence of signal charge in the pixel below 10^{-5}. So far two versions of the RD53 chip have been used by CMS: RD53A, a first prototype where three different analog front-end architectures were implemented, and RD53B-CMS, submitted in June 2017 and incorporating the latest design optimization and the linear front-end (FE) chosen by CMS. The RD53C (also known as CMS-ROC or C-ROC) is expected to be submitted in December 2022, and is intended to be the production design.

The readout chip is responsible for amplifying and digitizing the signals from the pixel sensors. The amplified signal is compared with a configurable threshold, typically tuned with a dedicated circuit where a well-known external charge is injected for a given pixel. The linear front-end implemented in RD53B provides a global threshold for the entire pixel matrix. Per-pixel differences in threshold can be accounted for by using trim bits that allow one to tune the per-pixel threshold within a configurable dynamic range with a 5-bit resolution. While typical pixel-to-pixel variations result in a threshold dispersion of hundreds of electrons, the trim bits allow one to reduce the dispersion to tens of electrons. The performance of such tuning in the RD53B chip is shown in Fig. 2, where a threshold of approximately 1100 electrons is achieved with a dispersion of 50 to 70 electrons, and an average noise around 130 electrons, for both planar and 3D geometries.

The readout chip is able to estimate the deposited charge in the sensor using the time-over-threshold (ToT) method with a resolution of 6 bits on the ToT, out of which only 4 bits are read out. The reduction to 4 bits is performed by either filling the 4 least significant bits only, or, by using a double slope mapping that keeps the full resolution in the first half of the 4-bit dynamic range while only a quarter of the resolution is kept in the second half, achieving an overall larger range. The

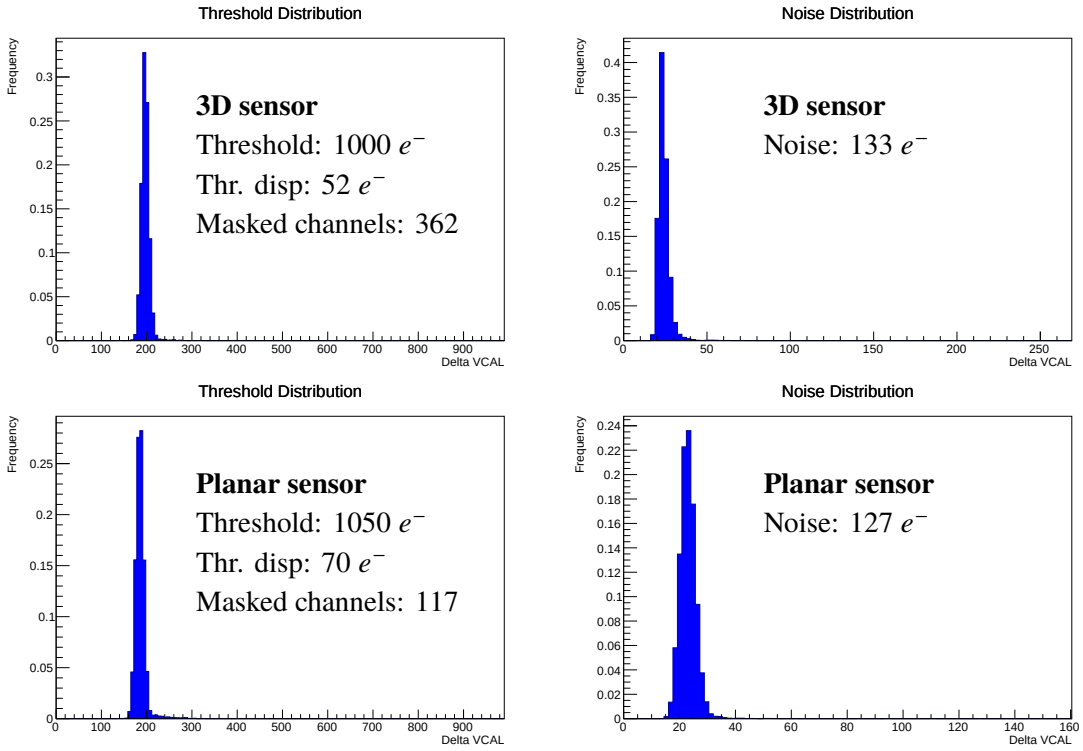

Figure 2: Results of the analog front-end tuning in a chip with a 3D sensor (top row) and a planar sensor (bottom row). Threshold distribution (left) and noise distribution (right) are shown for the full pixel matrix in VCAL units (1 VCAL unit corresponds to approximately 5 electrons).

dual slope ensures a good charge resolution where the collected charge is smaller - typically at the boundaries of clusters - while keeping a good dynamic range in order to provide a measurement of dE/dx for the identification of highly ionizing particles.

A data-merging functionality built into the chip allows merging of data from up to 3 neighboring chips into a configurable number of output lanes to drastically reduce the number of links and therefore material budget in regions where the occupancy is sufficiently low.

Another important feature incorporated into the chip design is a novel serial powering scheme. The power consumption of the chip is expected to be of the order of 0.7 $\mathrm{W\,cm^{-2}}$. Given this requirement, each module of the system cannot be powered in parallel without increasing the detector material budget above the system specifications, while DC-DC power converters cannot be used in the innermost layers of the detector either due to their limited radiation hardness. Because of this, the readout chip implements a powering scheme in which chains of up to 11 modules are powered in series. Each chain is supplied with a constant current, and a built-in shunt low-dropout voltage regulator feeds the chip with the necessary voltage, evenly distributing the power among the chips in the chain. The powering scheme poses a significant technical challenge, since it is the first time such a mechanism is used in a detector of this size, therefore this feature is being extensively tested. Powering chains with up to nine modules have been fully tested [4] obtaining good results, and preliminary studies with up to 12 modules look promising. The bias voltage of the sensor is provided in parallel to each sensor.

4. System readout and signal integrity

Hit data from the modules, as well as the command data sent to the modules, are transmitted through short electrical cables to a set of portcards, situated in the detector periphery, where the optoelectronics are located. Portcards are equipped with three LpGBT ASICs [5] and three VTRx+ optical transceivers [6], and are powered with DC-DC converters. Each portcard can drive up to three optical links at 10.24 Gb/s to the back-end electronics system situated outside the experimental cavern. Since the portcards are located at the detector periphery, radiation levels are reduced and it is foreseen that they will only need to be replaced once during HL-LHC running. Additionally, their contribution to the material budget is outside the detector tracking acceptance.

To test the performance of the readout system, a pseudo-random pattern of bits is sent from the chip to the back-end, where the received pattern is compared to the expected one. The rate of bits with errors is shown in Fig. 3 as a function of the `CML_TAP0_BIAS` register [3] of the RD53A chip, which controls the strength of the output signal driver. This register ranges between 0 and 1000, and a negligible number of errors is obtained below 320 (500) for the TBPX (TEPX) benchmarks, providing a significant margin for operation.

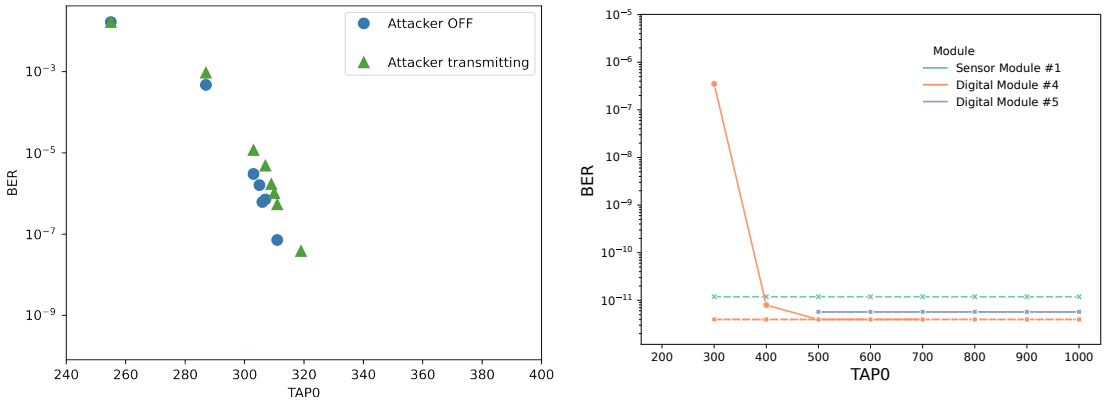

Figure 3: Bit error rate as a function of the `CML_TAP0_BIAS` register for TBPX modules under different scenarios of cross-talk (left) and for TEPX modules in different locations of the innermost ring (right) [4]. The cross-talk tests aim to quantify a potential signal quality degradation due to a near-by module (attacker) that sends a signal through a nearby cable. These tests show no significant degradation by cross-talk.

5. System mechanics

The detector mechanics is designed to be lightweight and simple, contributing minimally to the material budget and allowing the removal of the system for maintenance. It is built using lightweight carbon fiber with embedded stainless steel cooling pipes. The cooling is performed using a two-phase CO_2 circuit at -35 ° C, able to extract the 50 kW of power delivered to the whole system. The material budget is kept to a minimum in order to reduce the effect of multiple scattering. The expected interaction and radiation lengths of the detector material are shown in Fig. 4.

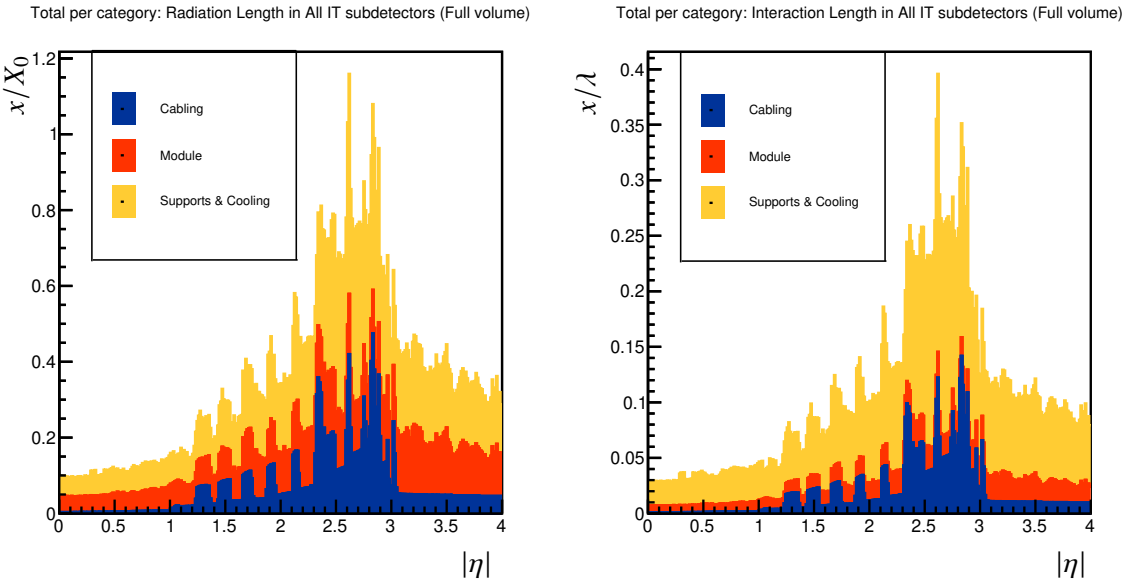

Figure 4: The expected material budget of the upgraded Inner Tracker estimated in units of radiation length (left) and nuclear interaction length (right).

6. Conclusions

The design and development of the CMS Inner Tracker for the Phase-2 upgrade of the experiment is at an advanced phase. The latest prototype detector modules are currently being tested and their performance is well within the specifications needed for them to endure the harsh conditions expected at the HL-LHC. In parallel, prototypes of the mechanics and cooling system have been produced and are being tested. Final prototypes will be available next year, after which detector construction will begin.

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