PROCEEDINGS OF SCIENCE

A truly cylindrical inner tracker for ALICE

Magnus Mager[a,*] **on behalf of the ALICE Collaboration**

[a] *CERN,*
Esplanade des Particules 1, Geneva, Switzerland

E-mail: Magnus.Mager@cern.ch

After the successful installation and first operation of the upgraded Inner Tracking System (ITS2), which consists of about 10 m^2 of monolithic silicon pixel sensors, ALICE is pioneering the usage of bent, wafer-scale pixel sensors for the ITS3 upgrade planned for Run 4. Sensors larger than typical reticle sizes can be produced using the technique of stitching. At thicknesses of below 50 µm, the silicon is flexible enough to be bent to radii of the order of 1 cm. By cooling such sensors with a forced air flow, it becomes possible to construct truly cylindrical layers which consist practically only of the silicon sensors. The reduction of the material budget and the improved pointing resolution will allow new measurements, in particular of heavy-flavour decays and electromagnetic probes. In this presentation, we will report on the sensor developments, the performance of bent sensors in test beams, and the mechanical studies on truly cylindrical layers.

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*Speaker

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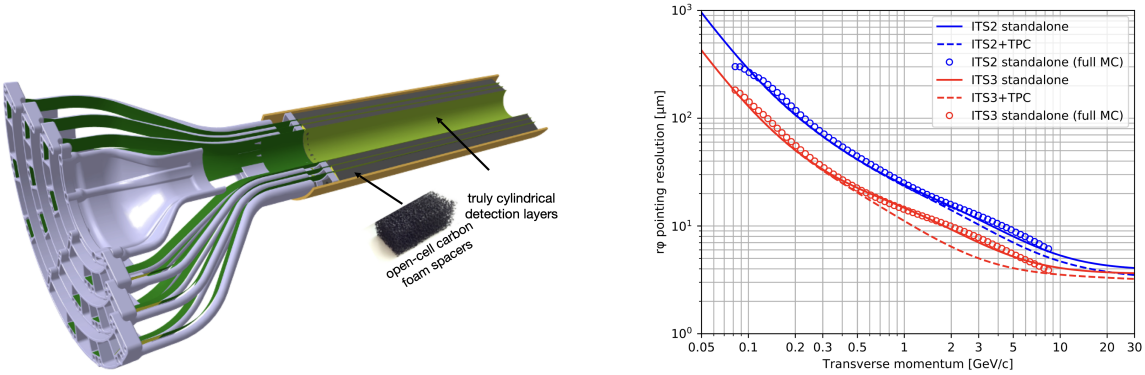


(a) Layout **(b)** Pointing resolution

Figure 1: Schematic layout of the ITS3 and its predicted performance.

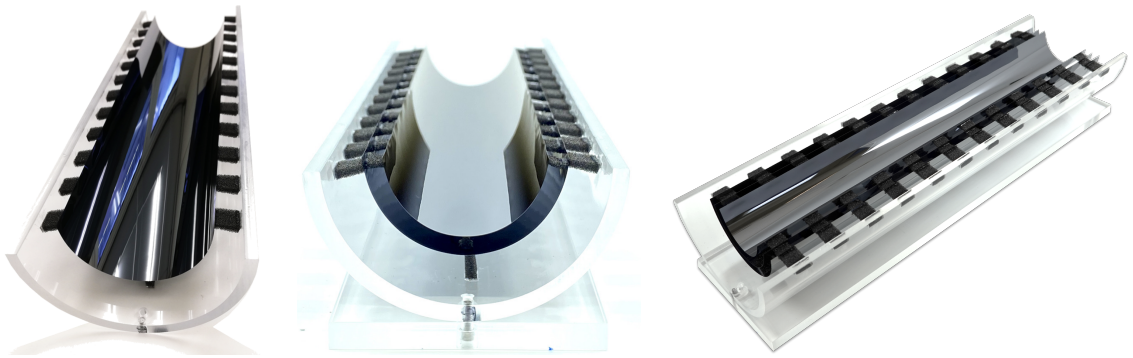
1. Introduction

ALICE is carrying out the R&D for replacing its inner-most three tracking layers during the LHC long shutdown 3 (scheduled for 2026–2028) [1]. For this new detector, "ITS3", ALICE develops a novel detector concept that is based on large-scale, flexible, fully integrated pixel sensors. This project entails a number of key innovations in the field of vertex detectors, notably including the development of wafer-scale ($O(10 \times 28\,\mathrm{cm}^2)$) CMOS sensors, bending of thin CMOS sensors to radii of down to 18 mm, as well as ultra-light mechanics based on carbon foam, and air cooling.

Figure 1 shows the baseline detector layout and the predicted improvement of pointing resolution with respect to the currently installed detector (cf. [1]). The layout is based on three layers with radii of 18, 24, and 30 mm and longitudinal extents of 28 cm. Each half layer is made of a single piece of silicon, a single "chip" including a large pixel matrix. This sensor also contains all electrical interconnections and hence eliminates the need of a supporting circuit board. The pixel matrix consumes little power, allowing for air cooling, while the detector periphery with the high-speed transmitters sits outside the detector acceptance where water cooling systems can eventually be used.

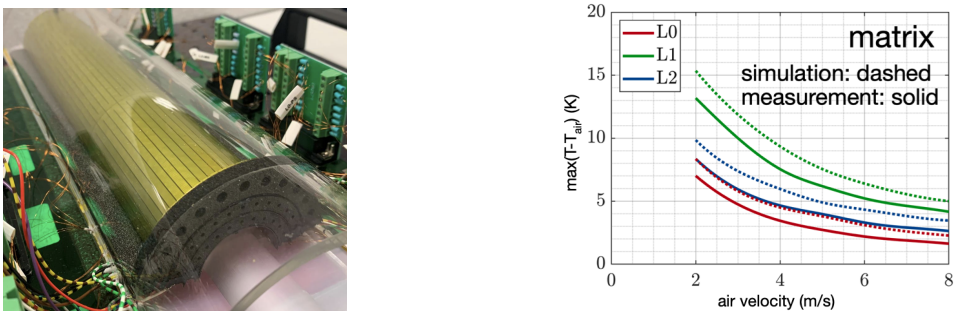
2. Mechanics

To assess the mechanical feasibility of a detector that is based on bent silicon sensors, and to develop and optimise the handling and assembly procedure, a number of prototypes have been built based on blank silicon wafers. Here, 40 and 50 μm-thick rectangular pieces from 300 mm unprocessed wafers were used. Figure 2 shows the assembly steps for a 3-layer assembly, starting from the outermost layer, and subsequently adding smaller radii. The resulting structures are characterised for material budget and off-shape distortions using 3D X-ray computer tomography (CT) scans. These scans showed a very good matching of the assembly to the ideal geometry. The periodic pattern of the supporting carbon foam wedges along z led to a periodic off-shape distortion of $O(100\,\mu\mathrm{m})$, and it was decided to replace the single wedges by bars covering the full length in the next iteration. The CT scans also revealed that glue was sucked into the carbon foam by capillary



(a) Layer 2 **(b)** Layers 1 and 2 **(c)** Layers 0–2

Figure 2: Assembly steps of "Engineering Model 1", based on dummy silicon.



(a) Setup **(b)** Measurement and simulation for the three layers (L0–L2)

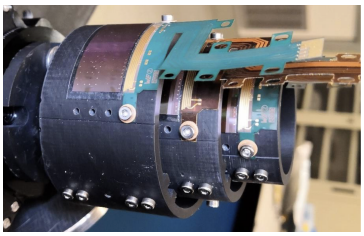
Figure 3: "Bread Board Model 1" based on flexible circuit boards, used for thermal studies.

action, leading to extra material budget at the chip-foam interfaces. This will be mitigated in future assemblies by applying a thin carbon foil between foam and sensor.

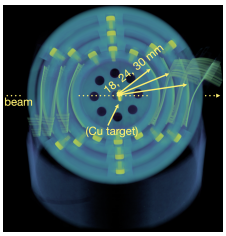
Parallel to the silicon assemblies, a model based on flexible circuit board was constructed (cf. Fig. 3a). It acts as a heating element and is used in a wind tunnel to measure the performance of air cooling and to tune the associated computer models (cf. Fig. 3b). From these first tests, it can be seen that moderate air speeds suffice to keep the temperature gradient over the sensor at acceptable levels.

3. Bent CMOS sensors

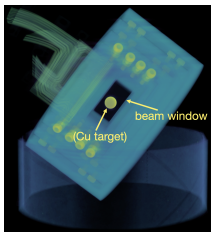
50 µm-thick ALPIDE chips, which are used to equip the current ALICE ITS2 [2, 3], are used to assess the feasibility and performance of bent CMOS sensors. First results from beam tests show that these chips function well after bending (cf. [4]), and more assemblies and tests are now done routinely. Figure 4 shows pictures from recent setups, called "µITS3", where three cylinders with radii of 18, 24, and 30 mm (matching the ITS3 design radii) are employed. Each cylinder can contain up to two chips. The chips are connected to flexible printed circuit boards using wire-bonding after bending. Underneath the central part of the chips, the jigs have an opening, where the chip is not supported. This allows shooting the particle beam through all chips without crossing extra material (cf. Figs. 4b, 4c).



(a) Setup (before final insertion)

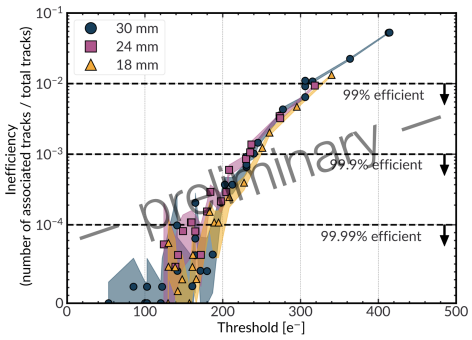


(b) X-ray CT (front)

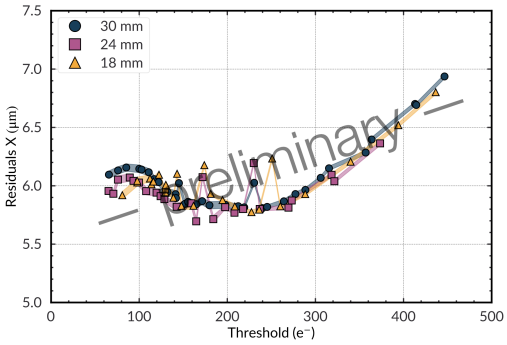


(c) X-ray CT (beam direction)

Figure 4: Photograph and X-ray CT scans of different µITS3 assemblies.



(a) Detection (in)efficiency



(b) Residuals (without subtracting telescope resolution)

Figure 5: Beam test results for ALPIDEs bent to different radii.

Figure 5 shows preliminary results of detection efficiency and spatial resolution for the three different radii. The performance figures are maintained at excellent levels (in particular detection efficiencies of ≫99 % at typical operating thresholds of 100 e), and no significant radius dependence is observed.

4. 65 nm CMOS prototype chips

The target baseline technology node for ITS3 will be the Tower Partners Semiconductor Co., Ltd. (TPSCo) 65 nm CMOS Imaging process. Together with CERN EP R&D [5], the ITS3 project evaluates this new technology for use as particle detectors in HEP applications. A first prototype run, containing 55 different prototype chips came back in summer 2021 and has been under detailed study since then.

Table 1 summarises the pixel test structures that are looked at in the

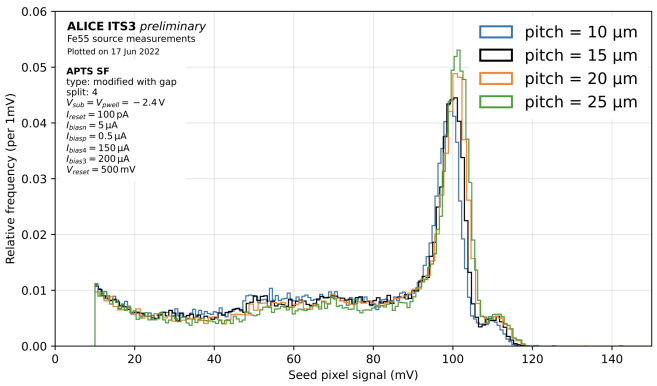


Figure 6: Seed pixel charge distribution for APTS sensors of different pitches when exposed to an Fe-55 X-ray source.

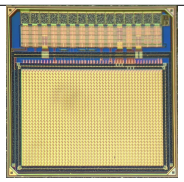
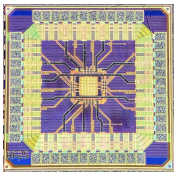
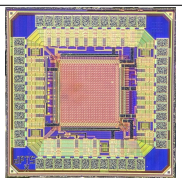
	CE-65	**APTS**	**DPTS**
			
matrix	64×32, 48×32	6×6	32×32
pitch (µm)	15, 25	10, 15, 20, 25	15
readout	rolling shutter, analogue	direct analogue (central 4×4)	asynchronous digital with ToT

Table 1: Pixel chip prototypes. Die size is 1.5×1.5 mm^2.

ITS3 context. They are produced in a number of variants to get a detailed understanding of the technology, and to select pixel pitches and circuits for both prototypes and final sensor.

The first two prototypes, CE-65 and APTS, feature an analog readout, allowing to get a complete understanding on the charge collection and sharing process. As an example, Fig. 6 shows the influence of pixel pitch, which is remarkably small. This is the outcome of a dedicated effort to optimise the electric fields similarly to [6, 7].

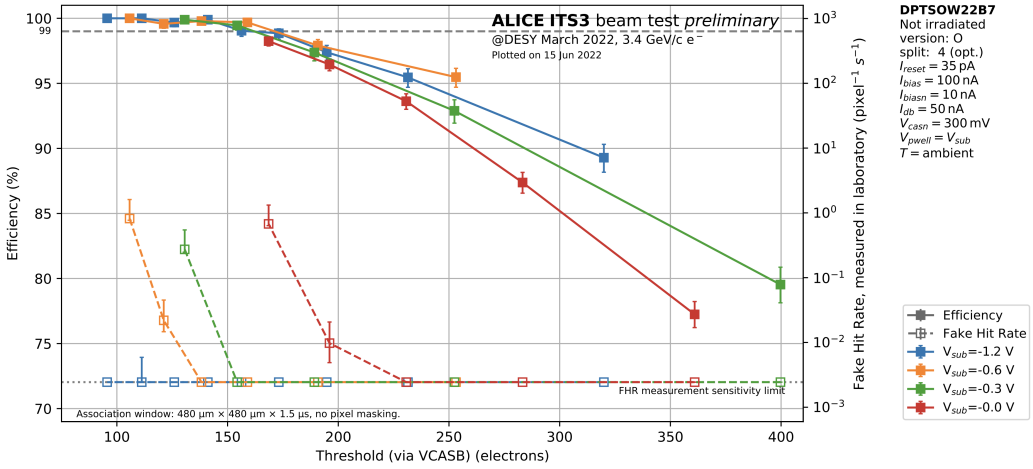
The DPTS chips contain pixels that have fully integrated in-pixel front-ends with amplification and discrimination. They are read out in an asynchronous fashion and provide time-over-threshold (ToT) information. DPTS chips were brought to numerous test beams and show excellent performance figures (cf. Fig. 7a). They were also tested after NIEL irradiation to the levels expected at ALICE ($\approx 10^{13}$ 1 MeV n_{eq}/cm^2), where they keep their performances. Even tests performed with doses that are 100 times larger (10^{15} 1 MeV n_{eq}/cm^2) show that the chip can still be operated at above 99 % detection efficiency (cf. Fig. 7b). Here it is worth pointing out that this result is achieved at +20 °C and not at cryogenic temperatures, which is an unprecedented result.

5. Summary and Outlook

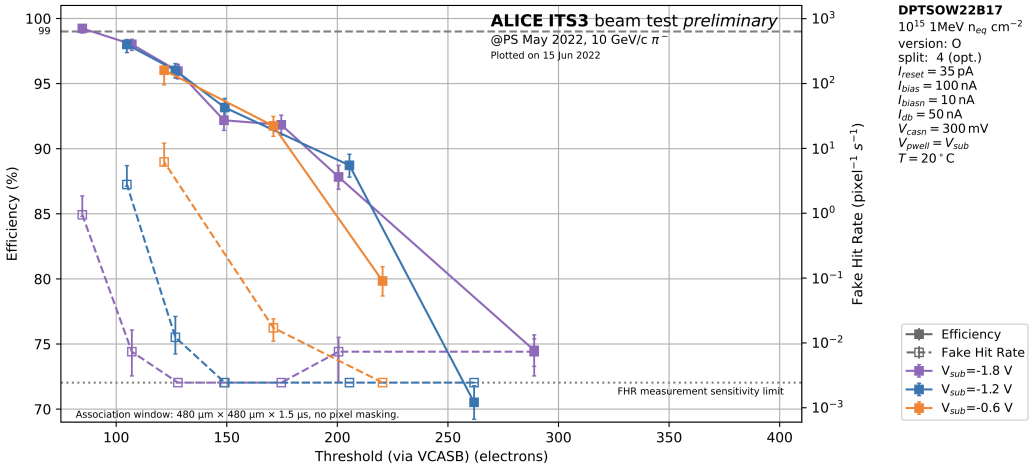
The ITS3 project has passed three major R&D milestones of: (1) mechanical integration of wafer-scale bent silicon chips; (2) in-beam demonstration of bent MAPS; and (3) qualification of the TPSCo 65 nm technology for HEP applications.

In summary, the results obtained so far are largely exceeding the ITS3 requirements and open up many future opportunities. Not only ultra-light (20 to 40 µm Si) high-resolution ($O(5\,\mu m)$) non-planar sensors are becoming a valid design option for precise vertexing, but also harsher radiation environments (10^{15} 1 MeV n_{eq}/cm^2 at +20 °C) can be addressed.

The project is now taking the next crucial steps towards the presentation of a Technical Design Report in 2023. In particular, the first stitched sensor covering the full length available on the 300 mm has been recently submitted for production, marking the start of a new era of large-scale CMOS sensors for particle detection. At the same time bending studies of processed chips from the 65 nm prototype runs are being carried out.



(a) efficiency and fake-hit rate vs threshold before irradiation



(b) efficiency and fake-hit rate vs threshold after NIEL irradiation to 10^{15} 1 MeV n_{eq}/cm^2

Figure 7: Beam test results of DPTS.

Acknowledgements

Some measurements (cf. Fig. 7a) leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

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