PROCEEDINGS OF SCIENCE

Full-system commissioning of TGC frontend electronics for Phase-2 LHC-ATLAS

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The Thin Gap Chamber system of the LHC-ATLAS is responsible for triggering muons in the endcap region at the hardware trigger stage. The frontend system of Thin Gap Chamber will be upgraded for HL-LHC to send binary hit-map at every Bunch Crossing to the backend system, where track reconstruction and p_{T} determination is performed to generate inputs to the Level-0 trigger. The new system incorporates improvements in Bunch Crossing Identification performance by fine-tuned clock distribution and capability of fine timing calibration. The Primary processor board is in charge of Bunch Crossing Identification and data transmission to the backend. An independent control module, named JTAG Assistance Hub, will take responsibility for FPGA configuration and clock phase monitoring of the Primary processor board with an SoC-based design. JTAG Assistance Hub also takes role in triggering the reconfiguration of frontend electronics for unrecoverable Single Event Upset errors by radiation effects. The timing calibration methodology for fine-tuning the clock phase and signal timing is realized with highly-extended flexibility in the Phase-2 system, exploiting the experience accumulated through the construction, commissioning, and operation of the existing Thin Gap Chamber system. System-level commissioning has been launched at KEK with prototypes of Primary processor boards and JTAG Assistance Hub and Amplifier-Shaper-Discriminator cards. The full-chain testbed system allows us to demonstrate fundamental functionalities of Trigger, Readout, Control and Calibration: clock phase fine-tuning, signal timing calibration, and hit readout with test pulse injection to Amplifier-Shaper-Discriminator cards with adjusted timing parameters.

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1. Introduction

The operation of the ATLAS detector [1] at the High-Luminosity Large Hadron Collider (HL-LHC) [2] will begin in 2027 for precision measurements of the Standard Model and to search for new physics with high statistics. At the HL-LHC, the peak instantaneous luminosity will reach $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which is more than three times higher compared to that of Run 3. This will pose challenges for the detectors, both in terms of high radiation and high pileup, with up to 200 interactions per bunch crossing. In order to efficiently collect events to explore the physics of interest in such a harsh environment, an extensive upgrade of the ATLAS detector and trigger and data acquisition system, denoted as the Phase-2 upgrade, is in progress. By extending the first stage trigger rate from 100 kHz to 1 MHz and increasing the latency from 2.5 μs to 10 μs, we can ensure a trigger system that has access to a variety of physics, with more sophisticated trigger algorithms. The first stage trigger in Phase-2 ATLAS experiment is called the Level-0 trigger.

Thin Gap Chamber (TGC) system of the ATLAS experiment is responsible for generating Level-0 trigger inputs for muons in the endcap region. TGC's Phase-2 upgrade [4, 5] involves the replacement of both frontend and backend electronics to satisfy the Level-0 trigger requirements. The schematic overview of the TGC Phase-2 electronics system is shown in Figure 1. The upgraded system consists of the primary processor boards (PS board) and JTAG Assistance Hub (JATHub) in the frontend and Sector Logic boards (SL) in the backend. Besides the digital components, the analogue Amplifier-Shaper-Discriminator (ASD) cards are mounted on the TGC detectors.

When muon passes through TGC, the detector generates an analog signal and the ASD sends discriminated hit signals to PS board. Then, the PS board aligns signal timing, and performs hit Bunch Crossing Identification (BCID). Next, the PS board sends a fixed-length binary hit-map to SL at every 40 MHz Bunch Crossing (BC). After that, the SL reconstructs muon track candidates and calculates p_{T} for each. Finally, the SL sends muon candidates to the down-stream trigger system and on acceptance of Level-0 trigger send readout data to the data acquisition system. JATHub is an independent control module and takes responsibility for FPGA configuration, debugging, error recovery and clock phase monitoring of PS boards.

TGC has 320k channels and each of the 23k ASD cards receives hit signals from 16 channels. Each of the 1 434 PS boards is connected up to 16 ASD cards. One PS board collects at most 256 channels and sends them to SL via two optical links of 8 Gbps for each. 29 PS boards are connected to one SL, and thus, each of the 48 SLs handles about 7 500 channels. There are 148 JATHubs in the TGC system, each connected to maximum 11 PS boards.

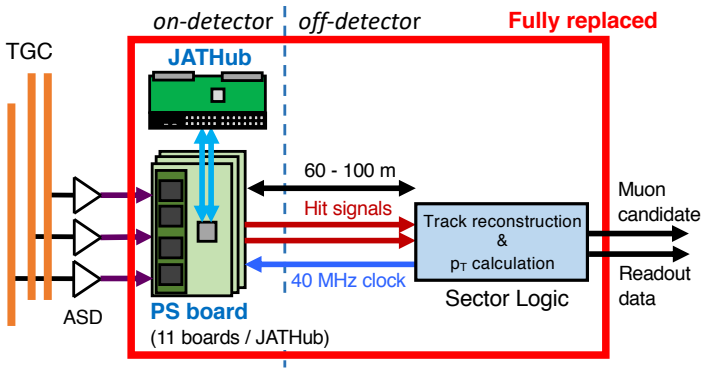
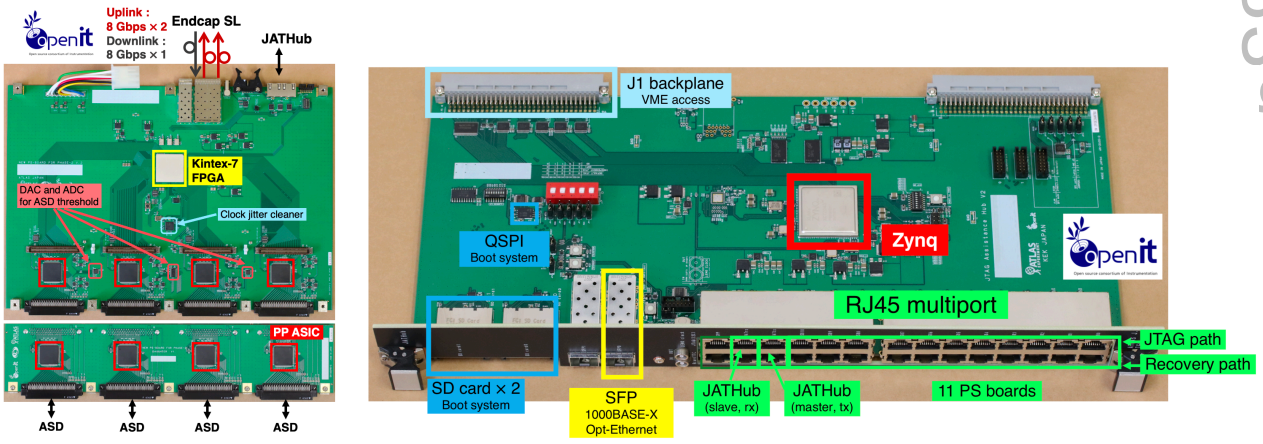


Figure 1: Schematic overview of the TGC Phase-2 electronics system

2. Development of the PS board

PS board is equipped with eight Patch Panel (PP) ASICs (four on mother board, four on mezzanine) and one Xilinx Kintex-7 FPGA [6], as shown in Figure 2 (a). One PP ASIC receives hit signals from two ASD cards. PP ASICs align the signal timing in units of ASD cards, exploiting variable delays available at the input stage to absorb differences in time of flight and signal cable length. BCID is performed by PP ASICs with a configurable gate-width. The variable delay and gate-width unit are controlled by a Phase Locked Loop (PLL) based circuit exploiting LHC clock synchronized to the bunch crossing. Then, the binary hit-map is sent to the PS board FPGA at every bunch crossing. PP ASICs also generate ASD test pulse which injects test charge to the ASD synchronously and simultaneously for validation of data readout chain and timing calibration.

PS board FPGAs receive 40 MHz LHC clock distributed from the SL via optical links and recovers the clock with fixed latency. The FPGAs align the clock phase with other PS boards within $O(100)$ ps precision, using the built-in PLL of the FPGA clocking resource, which is able to adjust the clock phase with a precision of 20 ps. An on-board clock jitter cleaner distributes the recovered LHC clock to PP ASICs, and provides the system clock for the FPGA operation and the reference clock to the serial link transmitters of the FPGA. Alignment of the LHC clock phase, provided to the PP ASICs in all 1 434 PS boards, enables the BCID gate-timing to be matched between PP ASICs, and the BCID gate-width to be kept as the minimum necessary length. Precisely aligned gate timing and small gate width ensure high probability of correct BCID while minimizing the chance of contributions from background that are out of sync with the proton bunch crossing timing, such as those originated from low-energy neutrons and photons. FPGA collects hit signals from the PP ASICs and transfers the 256-bit fixed-length binary hit-map at every bunch crossing to SL without data reduction via two optical links of 8 Gbps for each. Signal processing in the FPGA is done with a fixed latency regardless of the number of hits, and the data transmission to SL is performed with fixed latency relative to the collision timing. PS board also provides the threshold voltage to the discriminator in ASD cards, driven and monitored by DACs and ADCs. PS board FPGA controls ADC, DACs, PP ASICs, and clock jitter cleaner. All functionalities of the PS board have already been implemented in the prototype and tested as discussed in Section 4.



(a) The PS board prototype **(b)** The JATHub prototype

Figure 2: The prototype modules of TGC front-end electronics for Phase-2 upgrade. These modules are developed exploiting the intellectual property of the Open-It consortium [7].

3. Development of the JATHub

JATHub is a control hub module for the FPGAs on PS boards, equipped with the Xilinx Zynq-7000 System-on-a-Chip (SoC) device as shown in Figure 2 (b). The Zynq SoC integrates a Processor System including ARM-based processor with a Programmable Logic (PL) part equivalent to Xilinx 7-series FPGA and acts as the main driver of the frontend control system. One JATHub module is connectable to maximum 11 PS boards through category 6 cables, and 148 JATHub modules will control all 1 434 PS boards. JATHub has an Ethernet interface via optical fibers (1000BASE-X), exploiting built-in transceivers in the PL part of the Zynq. The PS part of the Zynq controls the JTAG signals for the configuration and debugging of FPGA on the PS board.

JATHub is responsible for triggering the reconfiguration of PS board FPGAs in case that unrecoverable Single Event Upset (SEU) errors happen in the configuration memory by radiation effects. PS board FPGAs run the Xilinx Soft Error Mitigation (SEM) controllers [8] to detect and recover SEU errors automatically. When the SEM controller observes an unrecoverable SEU error, the PS board FPGA asserts a recovery request signal to JATHub. Then, the JATHub initiates the entire recovery process based on the flash memory on PS board. JATHub is also responsible for recovering the neighboring JATHub.

For radiation damages in the storage device used for JATHub's booting, the JATHub system introduces redundancy in the boot procedure with a Quad SPI flash memory (QSPI) and two SD cards. Redundancy is introduced by having duplicated boot images in these devices. JATHub also has a role in monitoring the LHC clock phase of each PS board. By the in-situ measurement of the clock phases, JATHub assists the alignment of the recovered LHC clock phases between all PS boards, which is discussed in Section 2. All functionalities of the JATHub have already been implemented and tested as discussed in Section 4.

4. System-level commissioning of the TGC frontend electronics

For the system-level commissioning of the TGC Phase-2 frontend electronics, prototype modules of the PS board and JATHub are integrated in the test bench system at KEK. Figure 3 shows the schematic and photo of the test bench. Sector Logic module which is developed for the Run 3 system of LHC-ATLAS sufficiently emulates the SL for HL-LHC in this size of test bench. Optical links

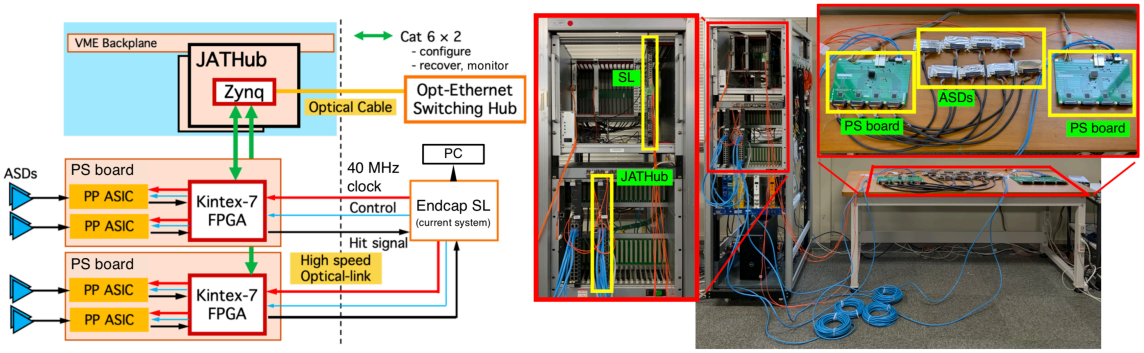


Figure 3: The schematic (left) and photo (right) of the test bench for system-level commissioning of the TGC Phase-2 frontend electronics. The test bench consists of the prototypes of the PS board and JATHub and the SL which is developed for the Run 3 system. SL and PS boards are connected by optical fibers, while JATHub and PS board are connected by category 6 cables.

between the PS board and SL are connected for the readout, register control, and clock distribution. Category 6 cables connect the PS boards and JATHub for the clock phase monitoring, the PS board FPGA configuration and recovery procedure. All necessary frontend components are already installed and all functions required for the operation and calibration can be tested in this test bench.

To prepare for the system test, we have developed and established the data format and protocol between the PS board and the SL, which carries data of hits and control commands. Then we demonstrated the register control in PP ASICs, ADCs, DACs, PS board FPGAs from SL. Three main objectives of the test bench are to demonstrate the fixed latency clock distribution, the clock phase measurement and adjustment, and the full-chain readout using ASD test pulse.

We have successfully implemented and demonstrated the fixed latency clock distributions to the PS boards via serial links between PS board and SL as well as the phase adjustment machinery. In order to verify these functionalities, we have developed the method to monitor the clock phase of each PS board by JATHub. JATHub measures the clock from the PS board 1 000 times at each phase with a minimum interval of 1/56 ns (~20 ps). By bypassing the build-in comma alignment function and 8b/10b decoder of the FPGA transceivers, fixed latency clock distribution was achieved. With 10 times of PS board reconfiguration, LHC clock phase variation less than the measurement granularity (~20 ps) was confirmed by JATHub.

We have demonstrated the clock phase alignment using two PS boards in a special setup with different fiber length chosen for each PS boards for the demonstration purpose. Figure 4 (a) shows the clock phases on two PS boards monitored by JATHub before phase alignment. Each red and black lines shows the phase of each PS board, and the timing difference of the clocks is observed as expected from the difference in fiber length. By shifting the phase of the clock on one of the PS boards by −829/56 ns in this particular case, the recovered LHC clocks of the two PS boards are aligned, which is confirmed by the clock phase measurement of JATHub as shown in Figure 4 (b).

Finally, we have demonstrated the entire readout chain using the ASD test pulse functionality that emulates hit signals from the TGC detector. Emulated hit signals are transferred in the readout

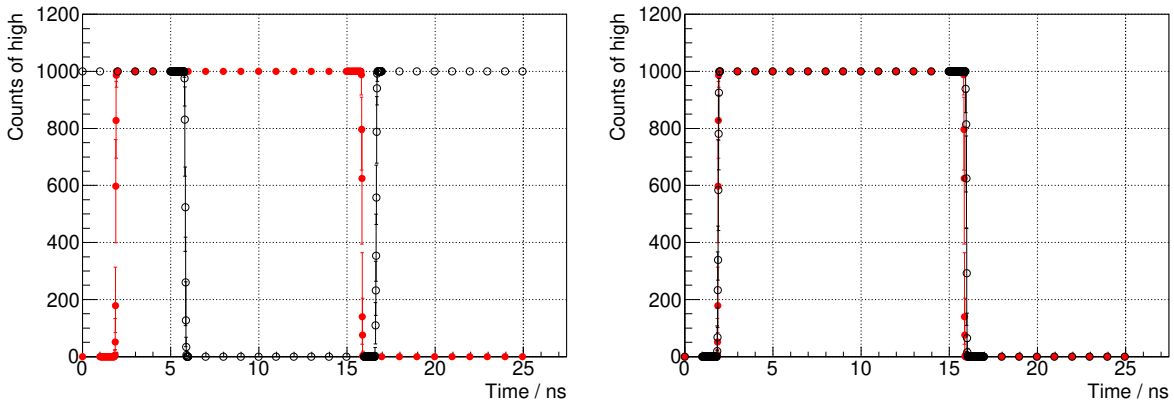


Figure 4: (a) Clock phases on two PS boards monitored by JATHub before phase alignment. JATHub measures the clock from the PS board 1 000 times at each phase with a minimum interval of 1/56 ns. Each red and black lines shows the clock phases on each PS board. (b) Clock phases on two PS boards after phase alignment. By shifting the phase of the clock on one of the PS boards (black line) by −829/56 ns in this particular case, phase matching of clocks with sufficient accuracy was achieved.

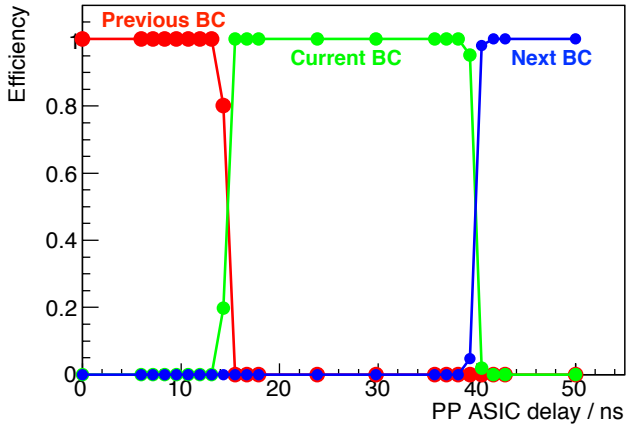


Figure 5: Delay curve showing the fraction of assigned bunch crossings as a function of PP ASIC signal delay. The input signals are identified to previous BC (red), current BC (green), or next BC (blue).

chain that consists of ASD, PP ASIC, PS board FGPA and SL, and are recorded with respect to the Level-0 Accept (L0A) signal. The hit data is dumped to the PC with well-adjusted ASD test pulse and L0A timing. We have achieved the fixed latency readout, and as a demonstration of the readout chain and the control from SL (especially the control of variable delays on PP ASICs), delay scan was conducted. Figure 5 shows the fraction of assigned bunch crossings as a function of PP ASIC signal delay, the so-called "delay curve". Each color means that input signals are identified to previous BC (red), current BC (green), or next BC (blue).

5. Conclusion

The TGC frontend electronics system will be upgraded for the HL-LHC, posing lots of unique challenges. With the well-tested prototype modules of the PS board and JATHub, the synchronized operation among the system components, the fine-tuned clock distribution, the calibration of the clock phase and timing parameters with fine accuracy, and the stable readout functionality are successfully performed in the test bench. Major functionalities and technologies of the Phase-2 frontend system have been developed and demonstrated. This successful demonstration of the system-level operation validates our operation and commissioning strategy for the new system for HL-LHC.

References

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