PROCEEDINGS OF SCIENCE

The HL-LHC Upgrade of the ATLAS Tile Hadronic Calorimeter

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The High-Luminosity phase of LHC, delivering five times the LHC nominal instantaneous luminosity, is scheduled to begin in late 2027. The ATLAS Tile Hadronic Calorimeter (TileCal) will need new electronics to meet the requirements of a 1 MHz trigger, higher radiation dose, and to ensure sound performance under high pile-up conditions. Both the on- and off-detector TileCal electronics will be replaced during the shutdown of 2025-2027. PMT signals from every TileCal cell will be digitized and sent directly to the back-end electronics, where the signals are reconstructed, stored, and sent to the first level of trigger at a rate of 40 MHz. This will provide better precision of the calorimeter signals used by the trigger system and will allow the development of more complex trigger algorithms. The TileCal upgrade program has undergone extensive R&D and beam tests. A "demonstrator" module has been tested in actual detector conditions. We present the results of these studies.

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1. Introduction

The ATLAS Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS detector at the Large Hadron Collider (LHC) at CERN. It was designed to perform the precise measurement of hadrons, jets, hadronically decaying tau-leptons and missing transverse momentum, as well as provide input signals to the Level 1 (L1) calorimeter trigger. As shown in Figure 1, TileCal is mechanically divided into four parts: two halves of the central long barrel (LBA and LBC) and two extended endcaps (EBA and EBC). Each of them is azimuthally segmented into 64 modules, giving a total of 256 modules. The modules are composed of steel absorbers and scintillating tiles. Figure 2 shows the structure of one TileCal module.

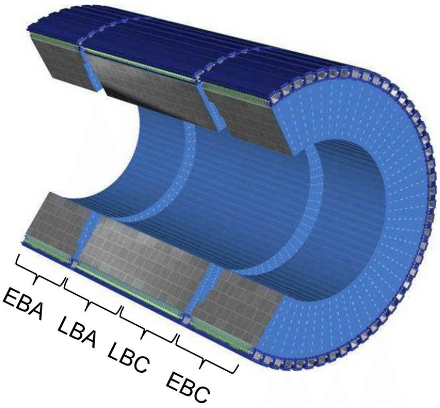

Figure 1: TileCal System

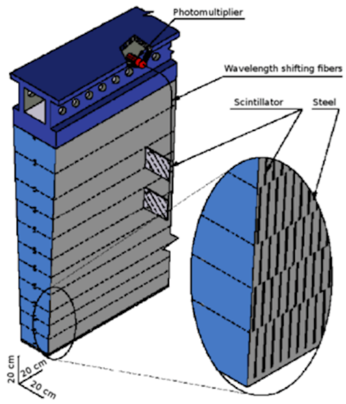

Figure 2: TileCal Module

The light produced by a charged particle passing through a plastic scintillating tile is transmitted to photomultiplier tubes (PMTs). Scintillating tiles are read out via wavelength shifting fibers coupled to around 10k PMTs. The readout of TileCal is grouped into pseudo-projective geometry cells, where each cell is read out by two PMTs. The modules in the long barrel have 45 PMTs, while the modules in the extended endcaps have 32 PMTs. The PMTs are housed in a mechanical structure called a super-drawer together with the associated electronics. The super-drawers are located at the outermost part of each module.

2. Upgrade of the ATLAS Tile Calorimeter

The High-Luminosity Large Hadron Collider (HL-LHC) will deliver instantaneous luminosities at least 5 times higher than the LHC nominal value, increasing the average number of collisions per bunch crossing to as many as 200. The resulting pile-up conditions, higher trigger rates and radiation dose are the main motivations for the upgrade of TileCal. The following sections describe the major changes to TileCal planned for the HL-LHC upgrade.

3. Mechanics

In the current system, the super-drawers consist of two 1.5 m long drawers with common power and read out. The new structure divides the super-drawer into four independently powered and read-out mini-drawers (MDs) that are each half the length of the current drawer. The expected benefits from implementing the MDs are easier access during the maintenance period and the ability to address issues. Each mini-drawer can house up to 12 PMTs equipped with the front-end amplifier/shaper cards, a Main board for control and digitalization, a Daughter board for high-speed communication, a high voltage distribution board and a low voltage power supply. The new structure fits very well with the modules in the long barrel where 45 PMTs are used. The modules in the extended endcaps have 32 PMTs and require less electronics. Due to this, the super-drawer for the modules in the extended endcaps are equipped with just 3 MDs, the outermost of which is mechanically extended by a pair of so-called micro-drawers (mini-MDs). The new layouts of the super-drawer for the modules in the long barrels and extended endcaps are shown in Figure 3.

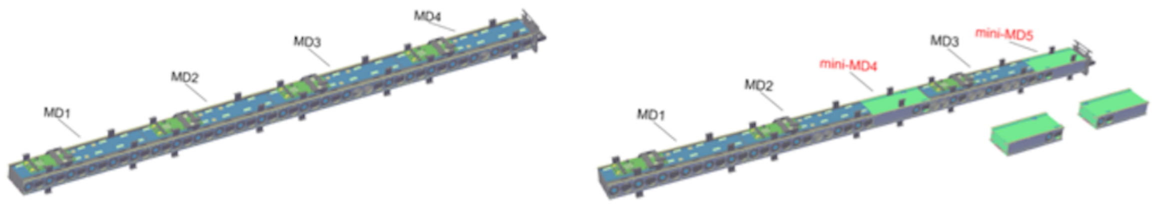

Figure 3: New super-drawer architecture for modules in the long barrels (left) and extended endcaps (right)

4. Readout electronics

As shown in Figure 4, the TileCal readout electronics is divided into front-end electronics (on-detector) and back-end electronics (off-detector). The following subsections describe the changes in electronics for the HL-LHC.

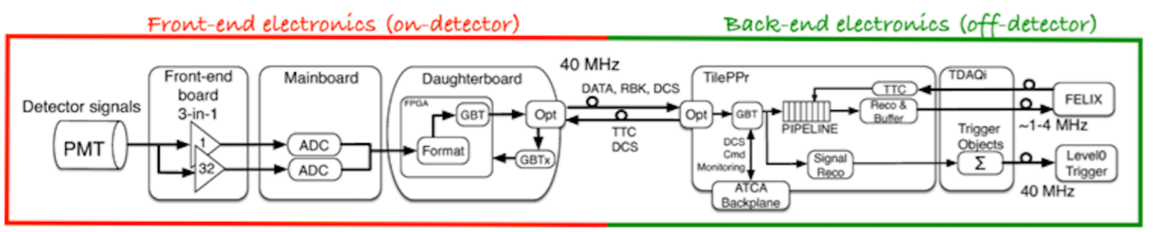

Figure 4: TileCal electronics for the HL-LHC

4.1 Front-end electronics

In the current system, the PMT signals are shaped, amplified, and digitized at 40 MHz using a clock that is synchronized with the beam crossing. The digital samples are stored in pipeline memories for the duration of L1 trigger latency (2.5 μs). In addition, analog sums of PMTs corresponding to projective trigger towers are produced and transmitted to the L1 calorimeter trigger system. The digital samples from events selected by the L1 trigger system are then transmitted to the Read-Out Drivers in the back-end electronics at an average rate of 1 kHz. For the HL-LHC upgrade, the PMT signals from all cells, after being shaped, amplified and digitized at 40 MHz, will be sent directly to the back-end electronics using optical fiber links running at 9.6 Gbps. The digital trigger sum will be created in the back-end electronics and sent to the Level 0 (L0) trigger system. This fully digital readout will provide a more granular and precise trigger system than the current design, and will also allow the development of more complex trigger algorithms. The main components of the new front-end electronics are discussed below.

PMTs covert the light to an electric signal and are being equipped with **active dividers**. The replacement of PMTs that have received the most radiation exposure is being done. Active dividers will be used instead of passive dividers to provide better linearity against a current in the PMT base.

Front-end boards (FENICS) are connected to the active divider outputs in the PMT blocks. Those boards provide shaping and amplification of the PMT signals as well test pulse generation and slow integrator circuits for calibration. There are two types of readout. The fast readout for physics operates in two different gains in order to cover a dynamic range from 200 fC to 1000 pC. The slow integrator readout integrates the PMT current for the calibration of the calorimeter using a ^{137}Cs source. It also provides a relative measurement of the accelerator luminosity at the ATLAS collision point. The front-end boards also inject a precise charge and measure the conversion from pC to ADC counts.

Main board receives the analog outputs from the front-end boards, digitizes them, and transmits the data in real time to the Daughter board. One Main board per MD digitizes the data from up to 12 PMTs. The fast readout uses 24 12-bit dual ADCs at 40 MSps, while the slow integrator readout uses 12 16-bit SAR ADCs at 50 kSps. The Main board routes the data to the Daughter board and provides digital control of the FENICS to configure it for physics or calibration.

Daughter board allows high-speed communication of 4.8/9.6 Gbps with the back-end electronics. It sends precision data but also slow control data and monitoring data of the front-end electronics. The Daughter board receives the LHC clock and distributes it to the front-end electronics, and exchanges configuration and control commands.

4.2 Back-end electronics

The PreProcessor is the core element of the back-end electronics. It receives the sampled PMT data from the Daughter board, calculates the amplitude and timing of the PMT pulses with digital filters, and sends digital trigger tower sums for every bunch crossing to the ATLAS trigger system. At the same time, the unprocessed data are stored in digital latency buffers to await a trigger decision. Data from triggered events are transmitted to the Front-End Link eXchange system (FELIX) for readout. By moving the latency buffers off of the detector and closer to the trigger system, the trigger propagation delay is greatly reduced in comparison with the current TileCal system.

5. Low Voltage System

The low voltage (LV) power distribution system provides power to the front-end electronics. Unlike the current 2-stage LV system, where different voltages are being provided to the front-end electronics by the LV box, the upgrade LV system consists of 3 stages. All LV power supply bricks convert the input of 200 V to provide 10 V to the front-end electronics, which is then converted by POL regulators to different voltages needed by the electronics. Monitoring of the bricks is done through the Detector Control System via ELMB (Embedded Local Monitoring Board), hosted by

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an ELMB mother board inside the LV box. The ELMB mother board has been redesigned to be compatible with the new 3-stage control system of the LV power supply bricks, and is very robust and radiation tolerant.

6. High Voltage Distribution and Regulation

The High Voltage (HV) system follows the design of the current system, with one single primary HV feeding an HV regulation board that regulates the individual HV for 32 or 48 PMTs. The HV regulation is done remotely from the USA15 cavern outside of the radiation environment of the detector. This increases the accessibility for maintenance but it also requires long cables. The validation of the long cables and remote regulation boards have been done in the laboratory and in test beams.

7. Test beams

Seven test beam campaigns were carried out at CERN from 2015 to 2018 with the aim to validate modules equipped with prototype electronics verification for the HL-LHC. During those campaigns, modules were exposed to different particles (muons, electrons, hadrons) and energies. Figure 5 (a) shows the expected response to hadrons in the experimental data (red circles) and Monte Carlo simulation (black squares) as a function of the beam energy. The distributions of the total energy deposited in the calorimeter obtained using electron beams of 20, 50 and 100 GeV are shown for both experimental (solid) and simulated (dashed) data in Figure 5 (b). The verification of the energy calibration is done to 2 % precision.

The response to muons as the ratios of the truncated means of the energy deposited in the layer A is shown in Figure 5 (c). The layer A achieved a uniformity of 1 % and a maximum data/Monte Carlo offset of 3 %.

8. Demonstrator in ATLAS

During the test beam campaigns, a demonstrator module that offers both backward compatibilities with the legacy modules (analog trigger signal) and the upgraded readout system (digital trigger signal), was tested. This module was fully inserted in the TileCal module LBA14 of the ATLAS detector at the end of July 2019. It is integrated with the ATLAS Trigger and Data Acquisition system as all the legacy modules. Good and stable performance with lower noise levels than the legacy modules has been found as shown in Figure 6. The project aims to gain experience with new electronics before the HL-LHC.

9. Conclusion

New conditions imposed by the HL-LHC require a redesign of TileCal which has been done based on the present rich experience. All the front-end and back-end electronics will be replaced for the HL-LHC, and the new readout structure will include a full digital readout and trigger. The tests of the design were performed during the test beams from 2015 to 2018. The demonstrator module

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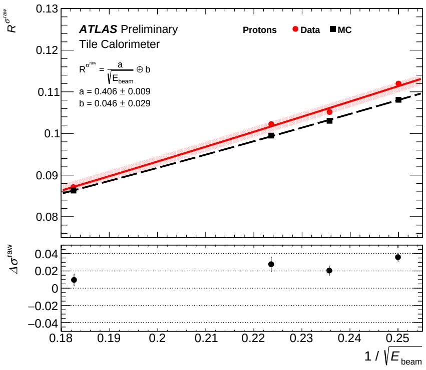
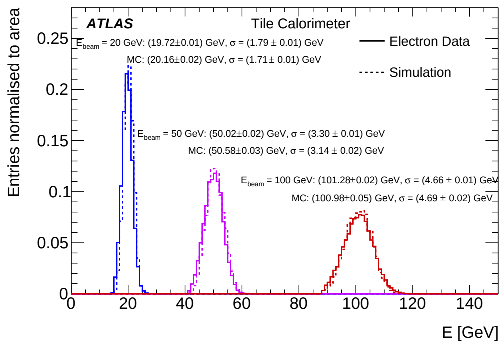
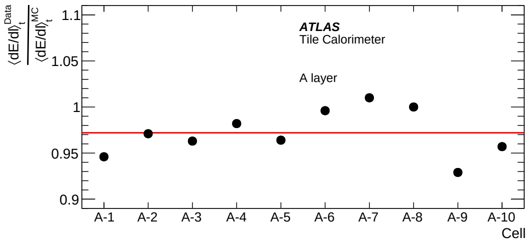


(a)



(b)



(c)

Figure 5: (a): the fractional resolution obtained with proton beams and simulation. (b): total energy deposited in the demonstrator with electron beams and simulation. (c): ratios of the truncated means of the energy distributions deposited in the A layer cell obtained using muon beams and simulation.

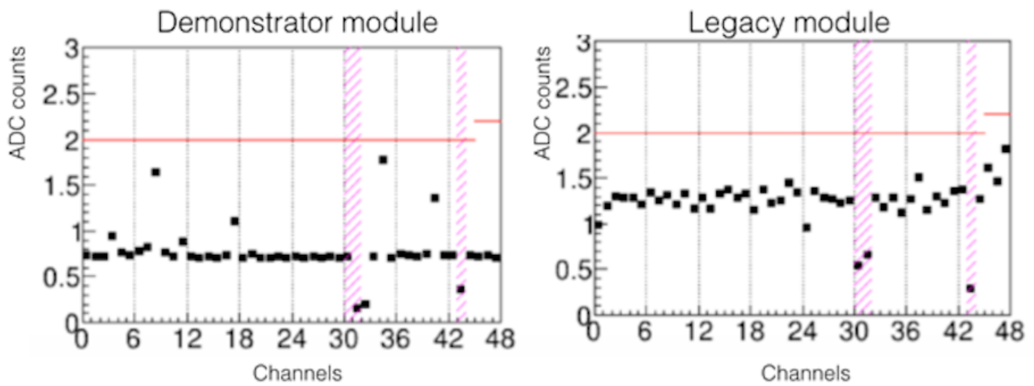


Figure 6: Noise comparison between the demonstrator (left) and the legacy module (right)

with the new electronics was inserted in the ATLAS detector in July 2019. It shows good and stable performance. Many components have entered into the pre-production or production phase.

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