PROCEEDINGS OF SCIENCE

The upgrade of the CMS Electromagnetic Calorimeter for HL-LHC

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The Electromagnetic Calorimeter (ECAL) of the CMS detector has played an important role in the physics program of the experiment, delivering outstanding performance throughout data taking. The High-Luminosity LHC will pose new challenges. The four to five-fold increase of the number of interactions per bunch crossing will require superior time resolution and noise rejection capabilities. For these reasons the electronics readout has been completely redesigned. A dual gain trans-impedance amplifier and an ASIC providing two 160 MHz ADC channels, gain selection, and data compression will be used in the new readout electronics. The trigger decision will be moved off-detector and will be performed by powerful and flexible FPGA processors, allowing for more sophisticated trigger algorithms to be applied. The upgraded ECAL will be capable of high-precision energy measurements throughout HL-LHC and will greatly improve the time resolution for photons and electrons above 10 GeV. The results in terms of performance achieved with a prototype system in a vertical integration test will be presented.

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1. Introduction

The electromagnetic calorimeter (ECAL) is part of the CMS experiment at LHC[1]. It has a fundamental role in the identification and reconstruction of photons and electrons, but it is also important for the measurement of jets and missing transverse momentum. It is a compact, hermetic, homogeneous, high-granularity electromagnetic calorimeter, composed of about 75 thousand lead tungstate ($PbWO_4$) crystals, distributed in a central cylindrical barrel (EB) and in two disks called endcaps (EE). The EB covers a rapidity region up to $|\eta| = 1.48$ and it is read out by avalanche photo-diodes (APDs), while the EEs extends the rapidity region up to $|\eta| = 3$ and it is read out by vacuum photo-triodes (VPTs). The crystals are $2cm \times 2cm \times 23cm$ in size and characterized by a density of $8.28gcm^{-3}$. Their short radiation length ($X_0 = 0.89cm$) allows the longitudinal shower containment within the crystal length, while the small Molière radius ($r_M = 2.19cm$) ensures lateral shower containment, making the calorimeter quite compact. The ECAL detector has been designed to have an excellent energy resolution, of a few percent for energy release above ~50GeV, and good time resolution, below 200ps for signals above 30GeV. Such performances contribute to excellent physics results, from the SM precision measurements to searches for New Physics (NP). However, ECAL was designed to meet these performance requirements up to an integrated luminosity of $500fb^{-1}$.
In order to maintain the current performances up to the integrated luminosity of 4500 fb^{-1} foreseen at the end of the HL-LHC program, several actions are required.

2. The ECAL upgrade for HL-LHC

During the HL-LHC period ECAL will have to run in a higher radiation environment. The transparency loss in EE will be so significant that the detector will be completely replaced by a new High Granularity calorimeter already before the start of the program. Moreover an increase in the APD leakage current is also expected, causing higher noise in the sensor. To mitigate this effect, the ECAL operating temperature will be reduced from the actual 18° to 9°C. From the point of view of the data taking, the HL-LHC program will provide an instantaneous luminosity of about $5\times10^{34}cm^{-2}s^{-1}$, implying an average number of concurrent interactions (pileup) per bunch crossing around 200 from the current 40. To maintain the same capability of distinguishing the primary vertices from spurious ones coming from the pileup an improved time resolution is required. Thus, a faster front end electronics is under development. This upgrade will give also the possibility to better distinguish genuine signals coming from electromagnetic showers in the crystals with respect to the faster anomalous signals generated by particles interacting directly with the APD (spikes).
The trigger rate will also increase to 750kHz from the current 100kHz. In these conditions, the new electronics must guarantee a maximum trigger latency of 12.5μs and provide the single crystal information already at the first level of trigger.

3. The new electronics for HL-LHC

3.1 The physics goal

To maintain the reconstruction performance during the HL-LHC conditions, ECAL must provide a time resolution of about 30 ps for energies higher than 50 GeV . In fact, from simulations, a pileup of 200 implies a reduction of primary vertex reconstruction efficiency of the 30% for the Higgs golden mode $H \rightarrow \gamma\gamma$. The vertex localization efficiency can be improved if a timing of 30 ps is reached. A 10% improvement in the fiducial cross-section sensitivity and $H \rightarrow \gamma\gamma$ resolution has been estimated, compared to the case when no precise timing is given [2].
The scheme of the new electronics [3] is shown in Figure 1. A board called Very Front End (VFE)

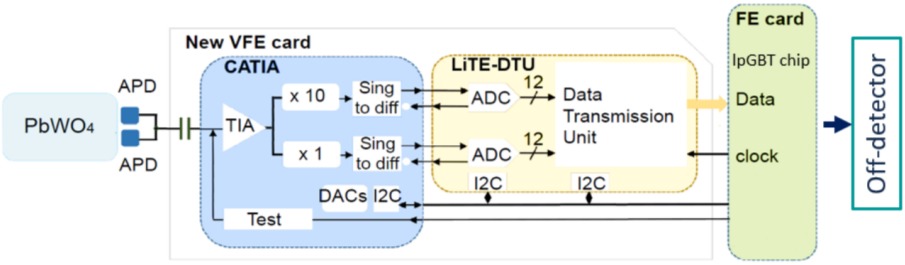


Figure 1: Scheme of the new ECAL readout electronics for the Phase 2 upgrade.

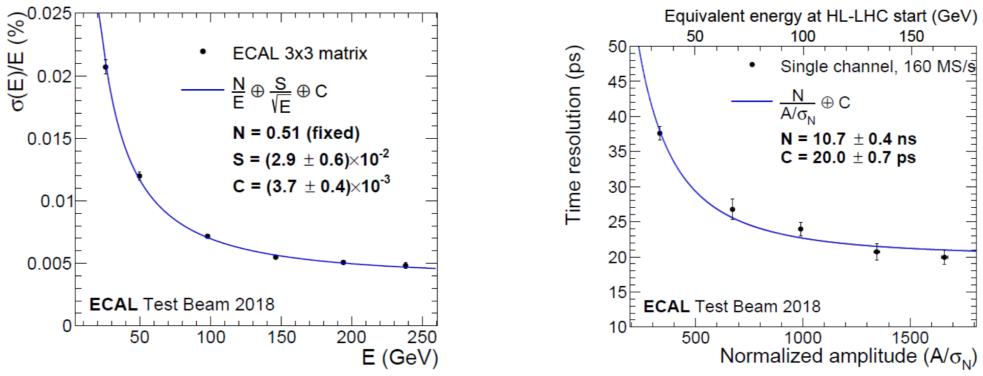
will host 5 Calorimeter Trans Impedance Amplifier (CATIA)[4] and 5 LIsbon-Turin Ecal Data Transmission Unit (Lite-DTU) chips.

3.2 The CATIA chip

CATIA is based on 130nm technology, connected to the APDs through kapton wires, with a bandwidth of 35MHz. It implements two outputs, one with gain x1 and the other with gain x10. This double-gain design allows to cover a range from 50 MeV to 2 TeV with the same device, selecting the appropriate output. The faster response of the CATIA with respect to the current amplifier guarantees better discrimination between the scintillation light and the spikes due to direct interaction in the APD.
Tests on the first version of CATIA, coupled with a commercial ADC, have been carried out at the H4/H2 beam line of the CERN SPS exploiting the electron beam of momentum between 25 and 250 GeV [5]. The obtained results are shown in Figure 2. The energy resolution matches with the current electronics performance, while the measurements on single crystals show that 30 ps time resolution can be achieved for electromagnetic showers with an energy greater than 50 GeV.
The outputs of CATIA are read out by LiTE-DTU chip.

3.3 The LiTE DTU chip

The LiTE-DTU is built in 65 nm CMOS technology and includes two 12-bit ADCs (one for each CATIA output) sampling at 160 MHz, designed by a commercial company and specified for



(a) **(b)**

Figure 2: CATIA energy resolution (a) and time resolution on a single crystal (b) obtained from the test beams at CERN [5].

an equivalent number of bits (ENOB) of better than 10.2 bit up to an input frequency of 80 MHz. It also includes a PLL circuit for clock generation, and a Data Transmission Unit (DTU).
The DTU selects the highest non-saturated gain channel and takes care of data transmission and compression.

In order to have the full signal shape sampled from the same CATIA output, meaning with the same gain of the amplifier, a look-ahead algorithm has been implemented in the LiTE-DTU. For this scope, two initial circular buffers have been designed, where the output of the ADCs is temporary stored. The buffer referred to the CATIA gain x10 output has an additional pointer that reads in advance the data to be transferred to the compression algorithm. If the sample in the reference position is saturated, the look-ahead algorithm opens a time window around that sample and during this interval only gain x1 samples are processed. The duration of the window increases as long as there are saturated samples.
Another requirement of the LiTE-DTU ASIC is to transfer every single ADC sample to the off-detector electronics through the low-powered Gigabit Transceiver (LpGBT). While the lpGBT link rate is 1.28 Gb/s, the transfer of the full ADC words at 160 MHz generates a 2.08 Gb/s occupancy. For this reason a lossless compression of the data samples has been embedded in the LiTE-DTU. The data compression algorithm is based on the fact that the energy spectrum in each ECAL crystal falls very rapidly, and the probability of having a particle releasing more than 2.5 GeV has been estimated from simulations to be at the order of 10^{-4}. Thus, the compression algorithm is designed to use only 6 bits to encode signals below 2.5 GeV, and 12 bits for signals above this threshold. One additional bit is used in the latter case to indicate from which ADC the sample is coming.
Finally, because the LiTE-DTU will be installed in a hard-radiation environment, it is designed to be TID (total irradiation dose) tolerant up to 20 kGy and the logic has been triplicated to be SEU-tolerant.
Several stand-alone tests of the first version LiTE-DTU have been performed in laboratory, to test the correctness of the compression algorithm and the performance of the ADCs. In figure 4 the ENOB

as a function of the input frequency is reported. The ADCs can be fed with the LiTE-DTU PLL or with an external clock generator, the Stanford CG635. Preliminary results show that the ENOB

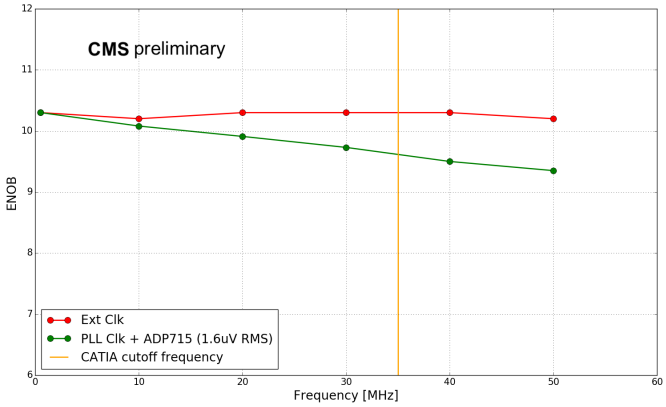


Figure 3: Effective Number of Bits obtained feeding the LiTE-DTU ADCs with the external clock generator Stanford CG635 (red curve) and with the LiTE-DTU PLL (green curve). The orange line shows the CATIA bandwidth cutoff.

value match the specification value up to the input frequency of 50MHz. The ENOB obtained using the internal PLL is around 9.7 bit at the CATIA cutoff, which is already sufficient. A new version of the LiTE-DTU chip has been in fact submitted in July 2021, implementing the last version of the PLL, which should guarantee a lower jitter and reduce the discrepancy.
The first version of the LiTE-DTU chips have been assembled with the CATIA chip on the new Very Front End boards; Preliminary results from the timing resolution obtained considering only the electronics (no crystals, no APDs connected) match very well the timing resolution required.

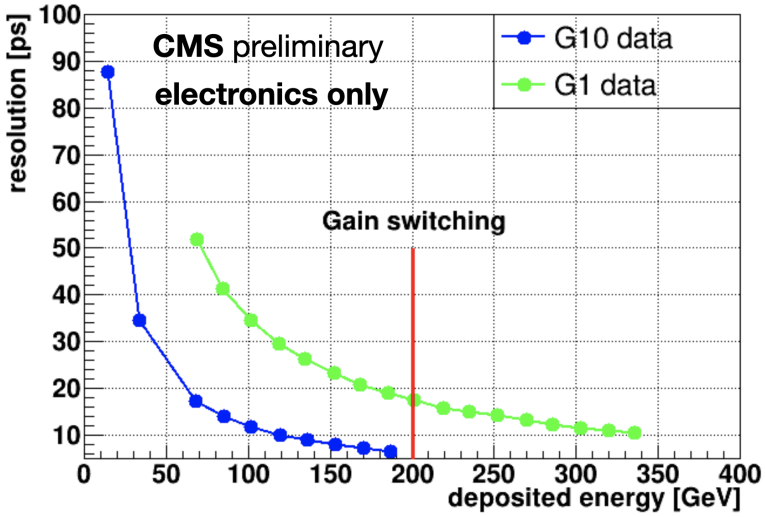


Figure 4: Timing resolution of Very Front End board assembled with both CATIA and LiTE-DTU. The result considering only the two chips match the requirements.

4. Conclusions

The upgrade of the CMS ECAL barrel calorimeter foreseen for High-Luminosity LHC was presented. The $PbWO_4$ crystals and APD photodetectors will be retained and will be operated at a temperature of 9C. The readout electronics will be replaced to cope with more pileup events, to maintain the current energy resolution, and to provide the needed much improved timing resolution. Preliminary tests of the new prototypes of the front-end components CATIA and LiTE-DTU show good performances. A new test beam, with the assembled Very Front End board was performed in July 2021 at CERN and the data analysis is ongoing. A larger scale test, with the electronics mounted on a complete ECAL module, is in preparation. The full production is foreseen in 2022 and 2023.

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