ATLAS towards the High Luminosity era: challenges on electronic systems

Carlos A. Solans Sánchez[a,*] **on behalf of the ATLAS collaboration.**

[a]*CERN,*
Esplanade des Particules 1, Meyrin, Switzerland

E-mail: Carlos.Solans@cern.ch

To maximize the physics reach, the LHC plans to increase its instantaneous luminosity to 7.5×10^{34} cm^{-2}s^{-1}, delivering from 3 to 4 ab^{-1} of data at $\sqrt{s}$ =14 TeV. In order to cope with this operation condition, the ATLAS detector will require new sets of both front-end and back- end electronics. A new trigger and DAQ system will also be implemented with a single-level hardware trigger featuring a maximum rate of 1 MHz and 10 μs latency. Enhanced software algorithms will further process and select events, storing them at a rate of 10 kHz for offline analysis. The large number of detector channels, huge volumes of input and output data, short time available to process and transmit data, harsh radiation environment and the need of low power consumption all impose great challenges on the design and operation of electronic systems.

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[*]Speaker

1. Introduction

In order to fully exploit the physics potential of the LHC with precision measurements of Higgs boson and SM properties (couplings, top mass, cross sections), search for beyond-SM signatures (Supersymmetry, new resonances, dark matter), and increase the coverage for rare physics events, the High Luminosity LHC (HL-LHC) is designed to deliver up to $4\,000$ fb^{-1} at a center of mass energy of 14 TeV with a peak instantaneous luminosity of 7.5×10^{34} cm^{-2}s^{-1}. The HL-LHC will become operational after the Long Shutdown 3 (LS3) expected to be around 2027.

For the ATLAS experiment [1], this means a Total Ionizing Dose (TID) above 10 MGy and a Non-Ionizing Energy Loss (NIEL) of 10^{16} 1-MeV-n/cm^2 in the parts of the detector closest to the beam pipe, where the usage of custom ASIC designs is expected, and a TID $\sim$ 100 Gy and 10^{14} 1-MeV-n/cm^2 NIEL in the outer regions, that will allow the use of more flexible FPGA designs combined with single-point-failure-free engineering. In both cases qualification against TID, including surface effects and transistor damage, and single-event-effects (SEE) including single event upsets (SEU) and single latch-up events (SEL) is required.

The upgrade of the ATLAS experiment consists of two Phases. Phase-I includes the installation of the New Small Wheel (NSW) A and C, new Barrel Inner Short chambers in sectors 7 and 8 of the Muon detector (BIS7/8), the upgrade of the Liquid Argon Calorimeter Trigger, and to the Trigger and data acquisition system [2] which is taking place during the Long Shutdown 2 of the LHC. The Phase-II upgrade that will take place during the LS3 will bring a new all-silicon Inner Tracker (ITk) up to $|\eta| < 4$ [3, 4], a new High-Granularity Timing Detector (HGTD) in the end-cap region [5], new muon chambers in the inner barrel region [6], data streaming at 40 MHz for the calorimeter [7, 8] and muon systems to off-detector readout and trigger electronics, and a new hardware Trigger [9]. Challenges to the electronics' systems include the implementation of the hardware Phase-II Trigger, the radiation hardness against SEE, and the shortage in silicon wafers. Unfortunately there is no way to control the latter, and in the following we will describe the ways to address the other two.

2. Phase-II Trigger challenge

The Phase-II Trigger system will be a L0-only hardware based Trigger at 40 MHz [9], equipped with feature extractors for Calorimeter and Muon systems that will be combined at a Global Trigger with improved acceptance and momentum resolution. FELIX [10] will be the read-out system for all systems for Phase-II, with a throughput of 290 GB/s (50 GB/s in Run2), and a total event size of up to 3.5 MB (2 MB in Run2), and a 3.2 GB/s recording rate (1.5 GB/s Run2). The Event Filter Trigger will provide high-level Trigger functionality using algorithms close to offline reconstruction and tracking methods. The options for the implementation of the Event Filter Trigger are Custom Associative Memories (ASIC design), commodity based on accelerators, commodity based on software only, or a full software design. The latest recommendation is to commit to a software solution. It is the strongest candidate except for the power consumption and cooling needs, and there is no real advantage to the custom solution, and it has smaller risk and a smaller short-term investment, and it allows to keep the options open for a heterogeneous solutions based on FPGA accelerators.

3. Challenges in the ITk

The ITk is an all silicon tracker to replace the current ATLAS inner detector. It is designed for extreme radiation tolerance, high granularity and low material budget. It extends the tracking coverage up to $|\eta| < 4$, and supports up to 1 MHz L0-only Trigger rate. The latest layout of the ITk [11] shown in Figure 1 is composed of 5 layers of hybrid Pixel detectors and 4 layers of Strip detectors in the central region, and up to 6 disks of Pixel and Strip detectors on both sides of the barrel. 3D-sensors with a pixel pitch of 100×25 μm^2 are used in the innermost barrel layer, and planar sensors with a pitch of 50×50 μm^2 in all other Pixel layers. The Strip detector is made out of 8 sensor types (2 barrel, 6 end-cap) with the Strips size ranging from 2 to 5 cm and a pitch of 75.5 μm.
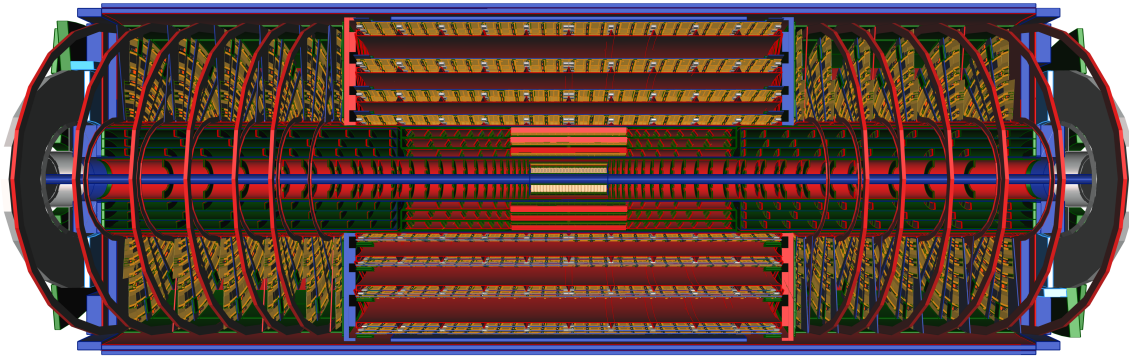

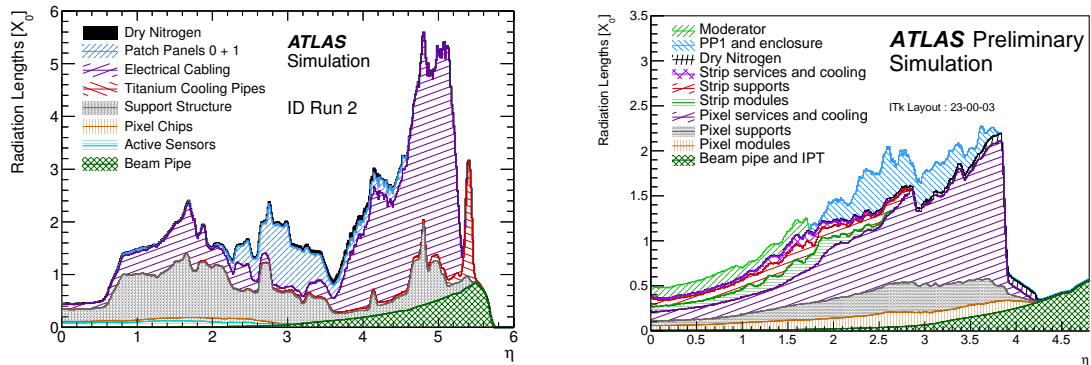**Figure 1:** Display of ITk Layout 23-00-03 [11]

Figure 2: Material distribution within the ITk volume in radiation lengths versus pseudo-rapidity $|\eta|$ for Run 2 (left) [3], and for the ITk Layout 23-00-03 (right) [11], broken down by sub-system and material category.

Material distribution within the ITk volume has been reduced as much as possible [11], with more than a factor 2 reduction in the forward region vs the current ID in Run 2 [3] as shown in Figure 2. Key features that contribute to this reduction include the usage of carbon-foam structures, capillary cooling distribution, rad-hard monitoring systems, and 10 Gb/s optical links in the whole of the ITk, point of load regulators as close as possible to the front-end in Strips, thinned sensors, and serial powering in Pixels.

The ITk will use the low power Gigabit Transceiver (lpGBT) [12] and the VTRX+ [13] Optical Link Module for data transmission. However in the Pixel case, in order to reduce the frequency of

SEUs, they will be placed outside of the detector volume, where 1 SEU per day per VTRX+ is still expected and mitigated by continuous monitoring. Additionally the Pixel modules require a custom Gigabit Receiver Chip (GBCR) [14] to recover the signal after the electrical transmission over 6 m of custom twisted pairs of data at 4×1.28 Gb/s. The measured jitter (peak to peak) at the output of the GBCR is 94 ps which is compatible with the requirements of the lpGBT. A cartoon of the on-detector data transmission chain is shown in Figure 3.
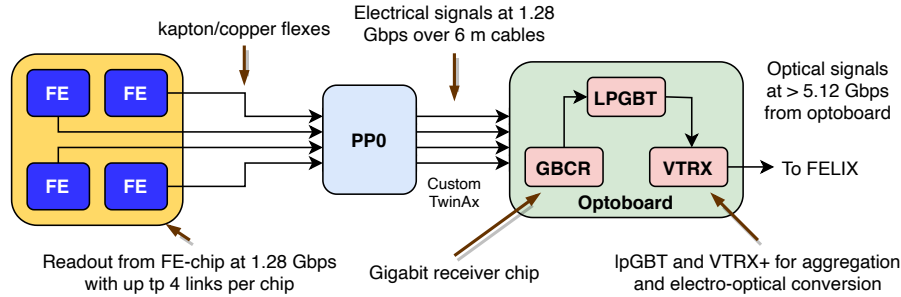
Figure 3: ITk Pixel data transmission

In the ITk Pixel, modules are powered in series by a constant current source, and monitored by a dedicated MOPS ASIC [15]. The ITk Pixel requires 912 serial powering chains, with a different number of modules ranging from 3 to 14. In a module, all four front-end ASICs are powered in parallel and regulated by 2 shunt LDOs (analog, digital). Tests are ongoing with RD53A [16] front-end ASIC prototypes to measure the minimum current required to power up all the modules in a chain. Tests with newer front-end prototypes will take place as they become available.

Mitigation against SEEs in the front-end ASIC designs in ITk is based on Triple Modular Redundancy (TMR) where a memory value is distributed to three different flip flops at write and the read value voted from the majority.

The ITk Pixel front-end ASIC is designed in TSMC 65 nm [17], and implements TMR in the pixel registers and in the global registers where it also includes temporal delay. The TMR is implemented by synthesis in the digital flow. It requires 40% more space than a regular flip flop. In the tests carried out at Louvain, no SEL has been observed, and the SEU cross-section has been measured to be σ(pixel) = 2-6 × 10^{-15} cm^2 for pixel registers, and σ(global) = 2-7 × 10^{-17} cm^2 for global registers. Since the rate of particles above the upset threshold is expected to be 500 MHz/cm^2, which is equivalent to an upset rate of 2× 10^{-5} Hz, or 1% of the pixels corrupted every 500 s, continuous reconfiguration will be used as a mitigation strategy.

Tests on the ITk Strips binary chip, ABCStar [18], were carried out with 480 MeV protons at TRIUMF and Heavy ions at Louvain. The recommendation was the re-design of the read-out ASIC, HCCStar, still under production. This included the removal of the now obsolete regional readout features, the replacement of the asynchronous resets by synchronous ones, and the triplication of the logic, the packet builder, and output path with the TMRG tool [19]. The redesign partially triplicated the control path, the input channels, and the registers. Functional simulations show good recovery in the non-TMR logic. Similar re-design for the monitoring and interlock ASIC, AMACStar, is being carried out.

4. Calorimeters

The upgrades in the Calorimeters target the sampling of the data at the bunch crossing rate (40 MHz) and to provide better energy resolution and more longitudinal information to the Trigger. This will be accomplished in the Liquid Argon Calorimeter by the end of Phase-I. The Phase-II upgrade will replace the front-end boards (FEB2), and introduce 2 ASICs in CMOS 130 nm, a full custom 14-bit ADC with successive approximation register architecture in 65 nm CMOS, and a calibration ASIC in HV-CMOS 180 nm. The mitigation strategies are the same as the ITk. The upgrade of the Tile calorimeter will introduce modular front-end mini-drawers with improved front-end linearity, complete redundancy from the cell to the off-detector electronics, and will combine TMR design with Xilinx Soft Error Mitigation tools for FPGA designs.

5. HGTD

HGTD will profit from the R&D from ATLAS, CMS, and RD50 to bring LGADs into a radiation hard environment with the aim to provide precision timing measurements in the forward region and contribute to luminosity measurements. Front-end modules are composed of 2 arrays of 15×15 1.3 mm^2 LGADs, and 2 ALTIROC ASICs, which are being designed in TSMC 130 nm technology. The first module prototypes are expected by the end of 2021. Their expected jitter is below 20 ps above 10 fC of collected charge, and their expected radiation hardness is 1.5 MGy TID and 2.5×10^{15}n/cm^2 NIEL. After characterization, SEE mitigation strategies similar to those of the ITk or the Calorimeters might be needed.

6. Muon systems

New MicroMegas and sTGC chambers have been installed during LS2 on the NSW and the BIS 7 and 8. One of the challenges is the use of the FEAST DC-DC converter expected to be radiation hard up to 200 MRad TID and 5×10^{14} 1 MeV n/cm^2 NIEL [20]. Another challenge is the usage of the GBTx 130 nm CMOS chips [21] for continuous read-out through FELIX, not because of its radiation hardness, but because the need for secondary GBTx chips in the chain accessible only through DCS which increases the risk for single point failures. Compensatory measures are the continuous monitoring and independent powering of the components.

7. Conclusions

The Trigger and DAQ challenge for HL-LHC is being addressed by the decision to run the Trigger at 1 MHz, with implications on detector readout and HLT processing, the focus on a L0-only Trigger, and the plan to use a commodity solution in High Level Trigger. Radiation hardness against SEE is addressed implementing robust enough designs against SEU and SEL which are specific to all ATLAS front-end ASICs including the CERN wide lpGBT. These are more relevant for ITk Pixel and Strip due to closeness to beam pipe. Finally the global semiconductor shortage is a challenge affecting production schedule and delivery dates for which there are no compensatory measures.

References

[1] ATLAS collaboration, *The ATLAS experiment at the CERN large hadron collider*, *Journal of Instrumentation* **3** (2008) S08003.

[2] ATLAS collaboration, *Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System*, Tech. Rep. CERN-LHCC-2013-018, ATLAS-TDR-023, CERN (Sep, 2013).

[3] ATLAS collaboration, *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, Tech. Rep. CERN-LHCC-2017-021, CERN, Geneva (Sep, 2017).

[4] ATLAS collaboration, *Technical Design Report for the ATLAS Inner Tracker Strip Detector*, Tech. Rep. CERN-LHCC-2017-005, CERN, Geneva (Apr, 2017).

[5] ATLAS collaboration, *Technical Design Report: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade*, Tech. Rep. CERN-LHCC-2020-007, CERN, Geneva (Jun, 2020).

[6] ATLAS collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*, Tech. Rep. CERN-LHCC-2017-017, CERN, Geneva (Sep, 2017).

[7] ATLAS collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter*, Tech. Rep. CERN-LHCC-2017-019, CERN, Geneva (Sep, 2017).

[8] ATLAS collaboration, *ATLAS Liquid Argon Calorimeter Phase-II Upgrade: Technical Design Report*, Tech. Rep. CERN-LHCC-2017-018, CERN, Geneva (Sep, 2017).

[9] ATLAS collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, Tech. Rep. CERN-LHCC-2017-020, CERN, Geneva (Sep, 2017).

[10] C.A. Solans Sanchez, *The FELIX detector interface for the ATLAS TDAQ upgrades and its deployment in the ITk demonstrator setup*, *Journal of Physics: Conference Series* **1525** (2020) 012033.

[11] ATLAS collaboration, *Expected tracking and related performance with the updated ATLAS Inner Tracker layout at the High-Luminosity LHC*, Tech. Rep. ATL-PHYS-PUB-2021-024, CERN, Geneva (Jul, 2021).

[12] S. Biereigel et al., *The lpGBT PLL and CDR Architecture, Performance and SEE Robustness*, *PoS* **TWEPP2019** (2020) 034.

[13] J. Troska et al., *The VTRx+, an Optical Link Module for Data Transmission at HL-LHC*, *PoS* **TWEPP-17** (2018) 048.

[14] C. Chen et al., *Characterization of a gigabit transceiver for the ATLAS inner tracker pixel detector readout upgrade*, *Journal of Instrumentation* **15** (2020) T03005.

[15] A. Walsemann et al., *A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector*, *PoS* **TWEPP2019** (2020) 013.

[16] RD53 collaboration, *The RD53A Integrated Circuit*, Tech. Rep. CERN-RD53-PUB-17-001, CERN, Geneva (Oct, 2017).

[17] RD53 collaboration, *RD53B Manual*, Tech. Rep. CERN-RD53-PUB-19-002, CERN, Geneva (Mar, 2019).

[18] W. Lu et al., *Development of the ABCStar front-end chip for the ATLAS silicon strip upgrade*, *Journal of Instrumentation* **12** (2017) C04017.

[19] S. Kulis, *Single event effects mitigation with TMRG tool*, *Journal of Instrumentation* **12** (2017) C01082.

[20] G. Ripamonti et al., *A 2.5V Step-Down DC-DC Converter for Two-Stages Power Distribution Systems*, *PoS* **TWEPP-17** (2018) 059.

[21] A. Caratelli et al., *The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments*, *Journal of Instrumentation* **10** (2015) C03034.