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Operational Experience and Performance with the ATLAS Pixel Detector at the Large Hadron Collider at CERN

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The ATLAS Pixel Detector is the innermost part of the ATLAS Detector at the Large Hadron Collider (LHC) at CERN. It is crucial for tracking and vertexing of charged particles originating from primary or secondary vertices and hence allows track reconstruction and particle tagging, utilised in the many analyses performed on ATLAS data.
The LHC has provided an excellent amount of data, leading to challenging conditions for the various subdetectors, which have to cope with an increased data rate and increased radiation damage. In this report, the operational conditions under those circumstances for the ATLAS Pixel Detector are discussed, followed by a brief discussion of some of the effects of radiation damage on the current detector. The challenges for the future, as well as the actions needed to ensure a stable operation, in the upcoming periods of data taking, are outlined.

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Introduction The innermost part of the ATLAS Detector [1] is the Pixel Detector [2], key to vertexing and tracking of charged particles originating from the interaction point or secondary vertices. In 2012, an additional innermost layer (the Insertable-B-Layer or short IBL) was introduced in the barrel section of the Pixel Detector, giving the detector a fourth barrel layer [3]. These four layers are completed by three layers of disks on both sides, providing further coverage in the end-cap regions.

The original three barrel layers of the Pixel Detector (referred to as the *initial* Pixel Detector henceforth), from the inside to the outside: the B-layer, Layer-1, and Layer-2, are located at radii of approximately 5 cm, 9 cm, and 12 cm away from the interaction point. The IBL was introduced at a radius of about 3.3 cm. This makes the IBL and then the B-layer most exposed to large amounts of radiation and the highest charged particle flux, giving rise to a harsh radiation environment and challenging data rates.

The challenge was enhanced by the excellent performance of the LHC. The instantaneous luminosity delivered by the LHC peaked at about 2×10^{34} cm^{2}s^{-1} during Run 2[1], twice its design value. While the IBL read-out chip (FE-I4) was designed to operate under such conditions, the outer layers and disks are comprised of pixel modules[2] with a read-out chip (the FE-I3) drafted for the lower, nominal conditions. FE-I3 modules are designed to operate up to a fluence of 10^{15} n$_{\text{eq}}$cm^{-2} and ionising dose of 50 Mrad. For the FE-I4 these design values are increased by a factor of five. For the FE-I4 the nominal pixel pitch was also decreased from the nominal 400 µm $\times$ 50 µm for the FE-I3 to 250 µm $\times$ 50 µm in the FE-I4. The FE-I3 pixel modules use n$^+$-in-n planar pixel sensors, whereas IBL has mostly also planar n$^+$-in-n sensors, but also n+-in-p 3D on the outermost modules. Not only the radiation hardness of the read-out chips was increased, but also of the sensors themselves. In particular, the IBL sets a precedence in the use of radiation-hardened 3D sensors in a high energy physics tracking detector at the LHC.

The entire tracking detector of the ATLAS Detector, including the current Pixel Detector, will be replaced during the High Luminosity Large Hadron Collider upgrade. This upgrade will take place after the Run 3 of the LHC. Run 3 will start in 2022 and last for three years, delivering up to 80 fb^{-1} per year. Given these boundaries, the Pixel Detector has to be operated and maintained up to this point, ensuring a reliable data acquisition and high data quality throughout Run 3.

Run 2 Operation and Radiation Damage To put the Run 2 operational conditions into numbers: The yearly delivered luminosity reached approximately 70 fb^{-1}, delivering a total of 160 fb^{-1} throughout Run 2. The average pile-up ($<\mu>$) peaked at above 60 interactions per bunch crossing. In addition, the level-1 trigger rate, i.e. the rate the pixel modules are triggered to be read-out, reached 85 kHz, depending on the trigger menu. The combination of these conditions leads to increased pressure on the data acquisition (DAQ) framework, in particular on the available data bandwidth for transmission of the data from the modules. To keep the bandwidth saturation low, modules were tuned to higher thresholds and very low charge hits were discarded. This effect can be see seen in Figure 1 where the different tunings are shown in various colours. ToT (time-over-threshold, i.e. the time the signal from an individual pixel cell stays above its discriminator threshold) corresponds to the cut on the detected charge, whereas the analogue threshold is the set

[1] Run 2 is the operational period of the LHC between 2016 to 2018

[2] A pixel module consists of a read-out chip and a sensor bulk, interconnected via bump bonds.

threshold within the amplifier stage of the pixel cell (i.e. the discriminator threshold value). In the plot, the occupancy, which correlates with the bandwidth usage, is shown versus the average pile-up. To validate that the impact of the higher threshold does not impact the performance, the tracking performance was closely monitored. Results of this are shown in Figure 2, where for the different tunings, the hit on-track efficiency is shown for the B-layer. For the 2017 tuning, a slight decrease in performance is visible for the most central (i.e. low track $|\eta|$)[3] region. This deterioration was mitigated by tuning the innermost modules of the B-layer to a lower analogue threshold ("*hybrid threshold*") in 2018.

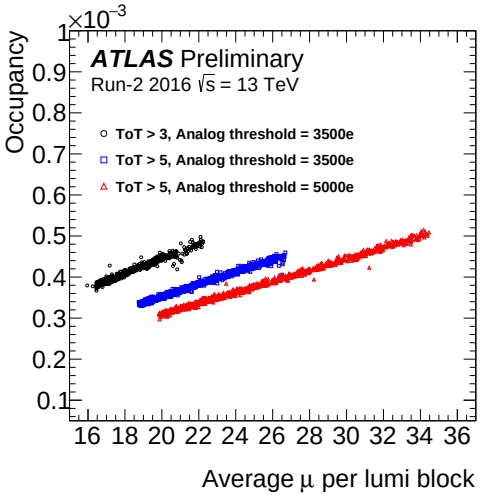

Figure 1: Occupancy versus <μ> [4].

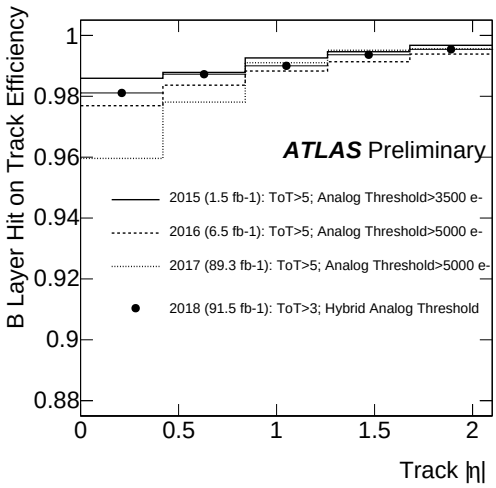

Figure 2: Impact on tracking performance [4].

With all the actions taken to limit bandwidth saturation, the Pixel Detector was operated with a desynchronisation error rate of less than 1% of the modules encountering such an issue in 2018. To achieve this, the read-out system for the initial Pixel Detector was progressively replaced by the new read-out hardware which was introduced for the IBL upgrade throughout Run 2. Moreover, the Pixel Detector introduced only a small dead-time of 0.2% into the ATLAS DAQ system. The data quality efficiency was at 99.5%, meaning that only 0.5% of the data collected were discarded, and hence not used in physics analyses, due to issues related to the Pixel Detector. For only 2018, the data quality efficiency was even at 99.8%, reflecting the fact that the system is constantly monitored and improved to en-

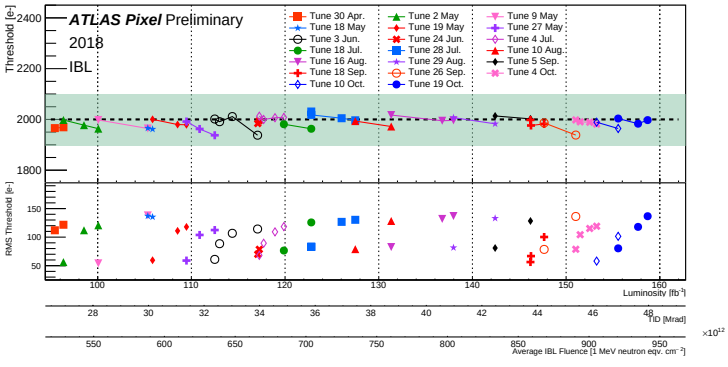

Figure 3: Tuning evolution with increasing radiation [4].

[3] $\eta = -\ln\left(\tan\frac{\theta}{2}\right)$, where θ is the polar angle measured from the beam (z) axis.

sure the collection of good data. Overall, less than 5% of the modules in the Pixel Detector are not operational, despite the age and harsh operational environment.

To sustain good data quality, the radiation damage, and effects due to it, have to be monitored, understood, and possibly mitigated [5]. One of the effects of the radiation is the total ionising dose effect on the FE-I4 [6]. The FE-I4 uses IBM 130 nm CMOS technology. The total ionising dose leads to a shift in the working point of the transistors. This causes the tuning of the modules to drift with increased ionising dose. For the threshold tuning, this results in a decrease in the threshold, as can be seen in Figure 3. Here the evolution of threshold with time is shown. A retuning approximately every 5 fb^{-1} keeps the threshold within 100 electrons (as indicated by the green band). While there is a systematic drift of the threshold, the equivalent noise charge remains constant with time. A drift is not only observed for the tuning of the threshold, but also in the tuning of the charge response. To ensure a uniform response, frequent retuning of IBL is needed.

Aside from the effects of ionising radiation also non-ionising damage poses a problem. Bulk damage leads to the trapping of charge carriers and hence an effective reduction of the collected charge. The evolution of measured average deposited charge per distance unit (<dE/dx>) and cluster size is studied. The evolution from 2016 to 2018 is shown in Figure 4 for the B-layer.

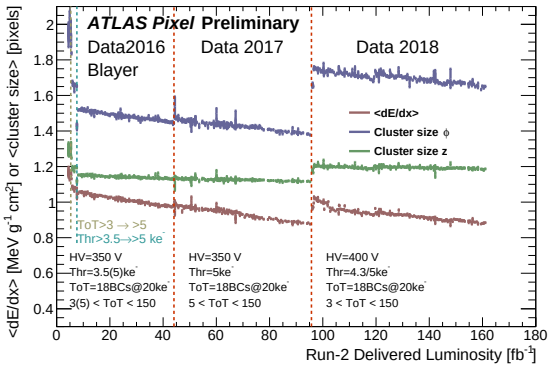

Figure 4: Evolution of <dE/dx> and cluster size [4].

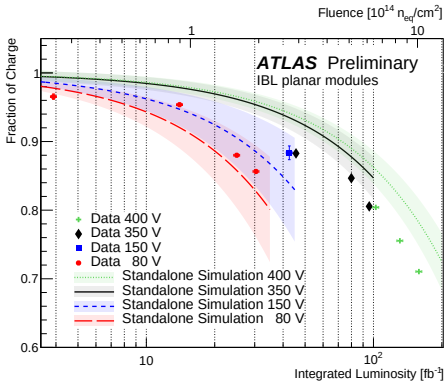

Figure 5: IBL charge collection efficiency [4].

At the beginning of 2016 a downward jump in both, <dE/dx> as well as cluster size, is visible. This was due to the increase of thresholds from 3.5 thousand electrons to 5 thousand electrons. Additionally, the lower cut on the charge was increased from three to five (ToT). This was done to prevent bandwidth saturation. From then onwards, a clear downward trend in <dE/dx> and in cluster size along the shorter pixel direction (ϕ) is visible. In 2018, the high voltage was increased from 350 V to 400 V and the thresholds were reduced to mitigate the effects of radiation damage. The most central modules were tuned to a threshold of 4.3 thousand electrons, and the low charge cut was decreased to three again. These actions increased the cluster size and measured <dE/dx> as seen by the upward jump.

While a small fraction of charge can be restored by increasing the high voltage, the best handle is to verify the possibility to tune the modules to lower thresholds. This need can also be seen in the evolution of the charge collection efficiency, which has been modelled and measured. The results for the IBL are shown in Figure 5, where the decrease in the fraction of collected charge decreases to approximately 70% at the current 160 fb^{-1} of integrated luminosity and radiation

damage thereof. Increasing the high voltage only slightly restores the collected charge. As of 2018, the most probable value for the amount of deposited charge for a minimally ionising particle (MIP) in a planar IBL module is ten thousand electrons with a tuning point of two thousand electrons. Lower threshold tuning points are currently being investigated for the upcoming Run 3.

Another quantity that is monitored and studied and heavily influenced by the radiation damage is the leakage current [7]. The leakage current can also be predicted by the Hamburg model [8]. In Figure 6 the evolution of the measured leakage currents for the IBL modules is shown throughout Run 2. The modules are split into different groups, depending on their position along the staves. This is because modules in the central region are subjected to a higher particle flux, hence experience more radiation damage. At two points, at about 40 fb^{-1} and just below 100 fb^{-1}, the measured and predicted leakage current curves dip. This is due to the scheduled technical stops at the end of the years and annealing during those periods. There is a systematic overprediction of the leakage current for all layers for high fluences.

In addition to the leakage current, deplete the sensor bulk is being monitored. This has been done by cross-talk scans before type inversion, and bias-voltage scans from then onwards. Knowing the leakage current and depletion voltage for full depletion is essential to predict how these values will evolve throughout Run 3. This is important to understand if these values will stay within the boundaries of what the power supplies can provide and what the services are rated for.

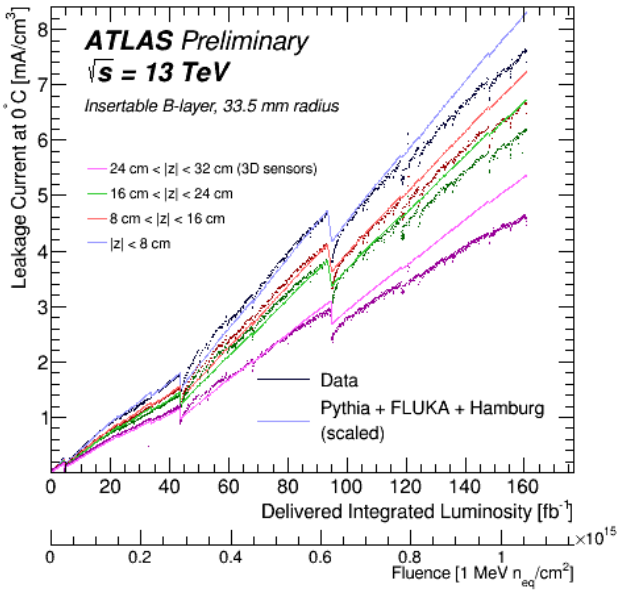

Figure 6: Evolution of leakage current for IBL in Run 2 [7].

To keep reverse annealing at a minimum, the detector is kept cold during the current long shutdown. Prolonged periods of reverse annealing would push the voltage required for full depletion beyond the maximum values that the services are rated for. With the current temperature history, the prediction of depletion voltage and leakage current for the IBL and B-layer stay below any system limitations. This gives confidence, that all the Pixel Detector modules can be operated fully depleted throughout Run 3.

During Run 2 a non-negligible amount of single-event upsets in the FE-I4 chip were observed. Single event upsets can induce bit flips in the registers of the chip. Depending on the register affected, this can for example detune a module and make it noisy, amongst many other effects. Overall, this not only introduces a problem because the module will not give the desired uniform response, but it can also change the low voltage current being consumed by this module. This can be seen in Figure 7 where an SEU corrupted a global register in the read-out chip around luminosity block 270. This caused the low voltage current to dip, as well as the hit occupancy on this module. The module was reconfigured five luminosity blocks later. The current and occupancy returned to

their nominal values. Fluctuations in the low voltage supplies are being closely monitored, as they can indicate problems with the modules.

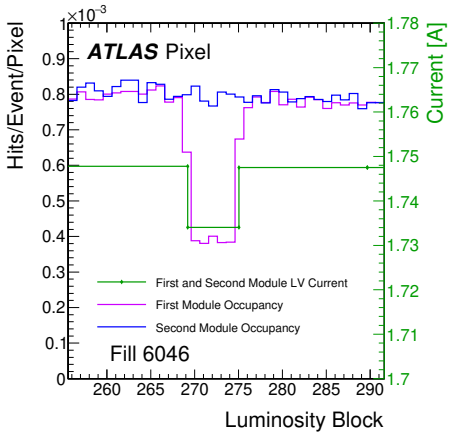

Figure 7: SEU in global IBL register [9].

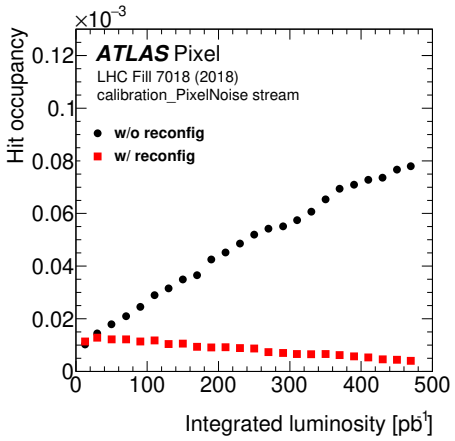

Figure 8: Impact of pixel register retuning [9].

To handle SEUs in the FE-I4 a mechanism to reconfigure the global registers was introduced during Run 2 [9]. This mechanism does not add any additional dead-time by exploiting the event-counter-reset (ECR) signal. The ECR signal is used for an ATLAS wide reset of various counters to ensure synchronisation. During the ECR there is a short time window where no triggers are issued. During this period, the reconfiguration of the FE-I4 global registers is issued. SEU of global registers can cause problems for the entire read-out chip, SEU of pixel registers can also cause problems in single pixels. This has also been observed by investigating the hit occupancy in two modules, one with a pixel register configuration enabled, and one where this feature was not enabled. The module without the reconfiguration got noisier and noisier throughout the run, a result of the detuning. The module with the reconfiguration did not observe this behaviour, but saw an expected decrease throughout the fill, as can be seen in Figure 8.

The time provided by one ECR signal is too short to fully retune all pixel registers. Hence a more sophisticated system was put in place. Unfortunately, this system was running on an unstable proprietary Kernel executed on a CPU on the DAQ hardware. During the extended shutdown between Run 2 and Run 3, a Linux kernel was deployed instead, and the full reconfiguration for global and pixel registers refactored and validated to run stable throughout Run 3.

Summary Throughout Run 2 the ATLAS Pixel Detector provided high-quality data with a data quality efficiency of 99.5% while only introducing a minimal dead-time of 0.2%. While the effects of radiation damage become more and more visible, mitigation strategies are developed and actions taken to ensure a smooth and stable operation during the upcoming Run 3 of the LHC.

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