PROCEEDINGS OF SCIENCE

Serial powering and signal integrity characterisation of the TEPX detector for the Phase-2 CMS Inner Tracker

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The CMS silicon pixel detector will be upgraded in anticipation of the High Luminosity LHC. The novel scheme of serial powering will be deployed to power the pixel modules and new technologies will be used for a high bandwidth readout system. In these proceedings, the new Inner Tracker Endcap Pixel Detector (TEPX) will be presented, with a particular focus on the concept to provide both power and data connectivity to the modules through a disk shaped PCB. As the TEPX also features the longest serial powering chains in the new Inner Tracker, results from serial powering measurements are presented.

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1. High-Luminosity LHC and the Phase-2 upgrade

The High Luminosity Large Hadron Collider (HL-LHC) [1] at CERN is expected to collide protons at a centre-of-mass energy of 14 TeV and reach the unprecedented peak instantaneous luminosity of 5–7.5 $\times 10^{34}$cm^{-2}s^{-1} – a factor five increase compared to the current, designed value. While this will allow the ATLAS and CMS experiments to collect integrated luminosities up to 3000 fb^{-1} during the project lifetime (2027–2040), the radiation level will be unprecedented (a 1 MeV neutron equivalent fluence of 2.3×10^{16} n_{eq}/cm^2 and a total ionizing dose of 12 MGy is expected at the distance of r ~25 mm, where r is the transverse distance from the center of the beam pipe). To cope with this extreme scenario the CMS detector will be substantially upgraded before starting the HL-LHC, a plan known as the Phase-2 upgrade.

2. Phase-2 upgrade of the CMS Tracker

The entire CMS silicon tracker will be replaced and the new detector will feature increased radiation hardness, a higher granularity, the capability to handle higher data rates and a longer trigger latency [2]. A sketch of one quarter of the Phase-2 CMS tracking system in the r–z view is shown in Figure 1. The Outer Tracker (OT) layout is shown in red/blue while the Inner Tracker (IT) layout in green/yellow.

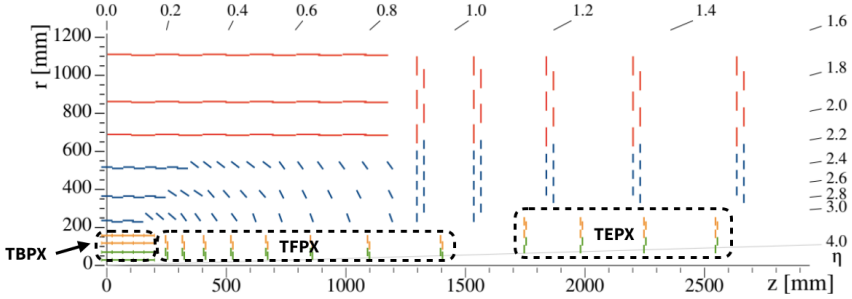

Figure 1: Proposed layout of the CMS Phase-2 Tracker

The upgraded IT will be composed of a barrel section, TBPX, and small and large forward disks, TFPX and TEPX respectively. The novel scheme of serial powering will be deployed to power the pixel modules and the Low Power GigaBit Transceiver (lpGBT) will be used to enable a high bandwidth readout system [3].

3. TEPX design

Figure 2 (a) shows the schematic design of the TEPX detector currently under development. It has four large disks on each side, extending the coverage up to $|\eta|$<4. Each disk consists of two half-disk structures with modules mounted on both the front and back sides. The half-disk is a three layer Polyimide PCB with 160 μm thickness as shown in Figure 2 (b) with modules arranged in five concentric rings. The pixel module comprises a pixel sensor (150 μm thickness, pitch 25 μm $\times$ 100 μm), four CROC (CMS ReadOut Chips) with 65 nm CMOS technology, a flex circuit, and a

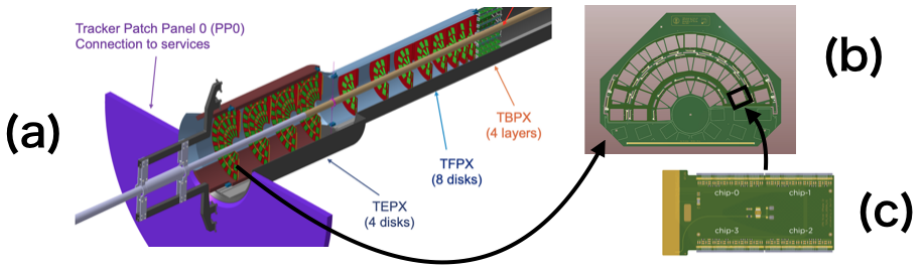

Figure 2: A diagram of (a) one quarter of the Inner Tracker, (b) the half-disk shaped PCB of the TEPX, and (c) a pixel module

mechanical support. The readout chips are bump-bonded to the sensors. A thin, high-density flex circuit, also referred to as high density interconnect (HDI), is glued onto the sensor and wire bonded to the readout chips. The HDI ships the data out, provides clock, trigger and control signals, as well as power distribution for the readout chips, and hosts all other passive and active components. Heat generated on the module is removed, via a layer of thermally conductive carbon foam, by pipes using a CO_2 evaporative cooling system. This keeps the pixel chips and sensors at an operating temperature of about -35 °C.

4. Serial powering and signal integrity testing

One primary focus now is to build up a realistic system with all TEPX elements in place (modules, readout electronics, cabling, serial powering) and understand differences of module behaviour when powered in series compared to standalone powering. This is particularly important for the TEPX system because it features the longest serial power chains in the entire IT.

Setup We assembled the chains corresponding to the innermost ring (Ring-1) with five pixel modules. The shortest (longest) trace length is around 85 mm (492 mm). After cooling down the system to an ambient temperature of -50 °C, we applied a digital (analogue) voltage of 1.3 V (1.2 V) for the prototype readout chip (RD53) [4] and tuned the front-end settings with a fully automated procedure.

Characterization of the pixel module In order to quantify the behavior of the module, we measured the efficiency as a function of injected charge, also known as an S-curve, as shown in Figure 3 (a). The efficiency is defined as the number of charge injection events with a pixel hit detected, divided by the number of charge injection events. Using this S-curve, two quantities are extracted; the "spread" of the S-curve where the efficiency is 50%, called the threshold distribution shown in Figure 3 (b), and the slope of the S-curve obtained by applying a fit using an error function, called the noise distribution shown in Figure 3 (c). Comparison plots of these quantities with and without serial powering are shown in Figure 3 (d) and 3 (e).

Although a slight degradation of the threshold distribution is observed, the difference is up to ~40 e in terms of the spread. This is small compared to the typical threshold value of 1900 e and should not cause any difference in practical operation. No degradation is found for the noise distribution. The next step will be to continue to extend the chain by adding further modules,

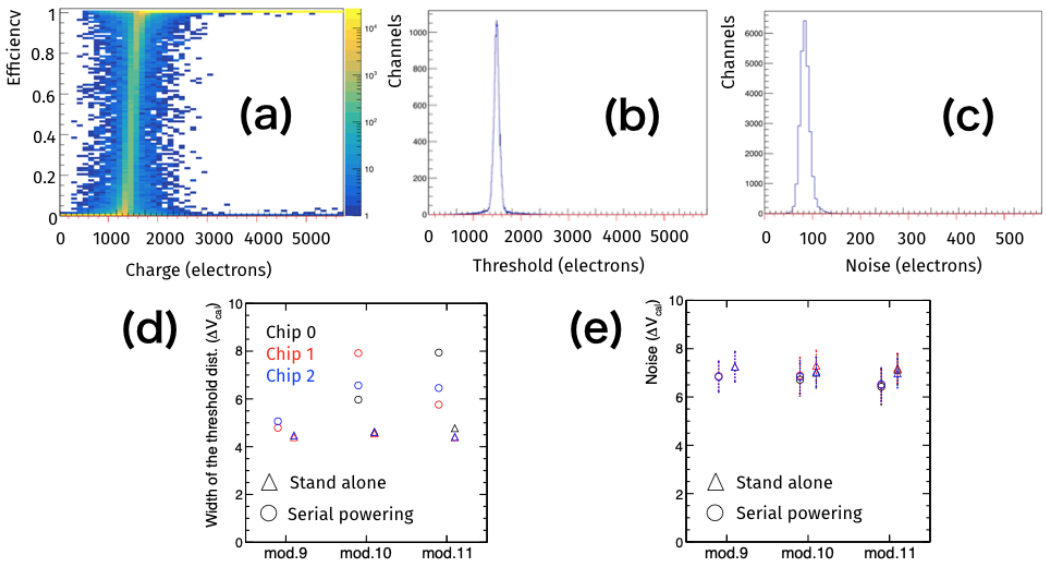

Figure 3: Characterization of the module; (a) The pixel hit efficiency for all pixels as a function of injected charge, called an S-curve, (b) projection of the S-curve onto the x-axis at 50% efficiency, (c) steepness of the turn-on curve, (d) width of the threshold distribution, and (e) mean and RMS of the noise distribution. Three representative modules are shown. Chip 0,1,2 represents the chip ID within the pixel module.

including sensors, to study the HV distribution, as well as verifying the serial operation of the longest chain in Ring 5, where twelve modules are located.

5. Summary

A new pixel detector is being designed for CMS in preparation for the High Luminosity upgrade of the LHC. The new layout features extended coverage in the forward region known as the Tracker Endcap Pixel Detector (TEPX). A realistic setup consisting of all the elements required for testing a serial powering chain has been assembled. The performance of the pixel modules in the disk, while being powered in series, has been compared with the one achievable in stand-alone. No degradation was observed in terms of the noise level and it was possible to establish simultaneous reliable communication to all modules for the first time.

References

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