

# Optimisation of the CMS Tracker Endcap Pixel Detector as a precision luminometer and background monitor at the HL-LHC

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The High Luminosity upgrade of the LHC (HL-LHC) places unprecedented requirements for background monitoring and luminosity measurements. The CMS Tracker Endcap Pixel Detector (TEPX) will be adapted to provide high-precision online measurements of bunch-by-bunch luminosity and beam-induced background. The implementation of dedicated triggering and readout systems, the real-time clustering algorithm on an FPGA and the expected performance are discussed. The innermost ring of the last layer (D4R1) will be operated independently from the rest of TEPX enabling beam monitoring during the LHC ramp and during unqualified beam conditions. The system optimisation and the dedicated timing and trigger infrastructure for D4R1 are also presented.

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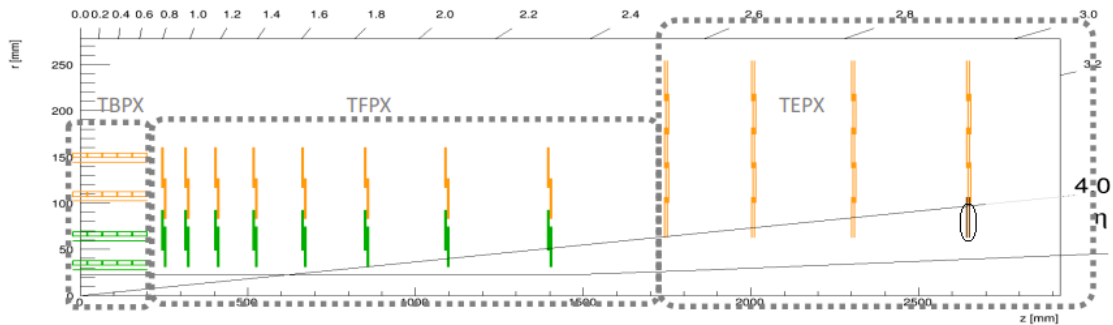
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## 1. THE CMS PHASE II INNER TRACKER

The High Luminosity (HL-) LHC will increase instantaneous luminosity to an unprecedented value of  $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$  which corresponds to 200 proton-proton collisions per bunch crossing (pileup). The Run 2 CMS [1] tracker will be replaced to handle the extreme radiation environment and charged particle track reconstruction challenges at high pileup. CMS Phase II Inner Tracker as shown in Fig. 1 will consist of four barrel layers (TBPX), as well as eight forward disks (TFPX) and four endcap disks (TEPX) at each side of CMS. Each TEPX disk will comprise of five rings having 20, 28, 36, 44 and 48 modules respectively. TEPX will be used for tracking as well as luminosity measurement. It will have better radiation tolerance, increased granularity, improved two-track separation, and extended tracking acceptance to  $|\eta| = 4$ . Hit occupancy per pixel for TEPX will be less than 0.1% to ensure excellent tracking performance under high pileup conditions. The design will also ensure that the pixel cluster counting (PCC) method, used for luminosity determination, will be linear with pileup and have high statistical precision. Disk 4 Ring 1 (D4R1) is located at 2.65 m away from the interaction point. It is beyond the tracking acceptance ( $|\eta| = 4$ ) as this region has few tracking points. It can thus be solely used for the purpose of luminosity measurement, operated as an independent luminometer.



**Figure 1:** Layout of CMS Phase II Inner Tracker showing the barrel, forward and endcap regions. The black circle shows the first ring of the last TEPX disk (D4R1) [2].

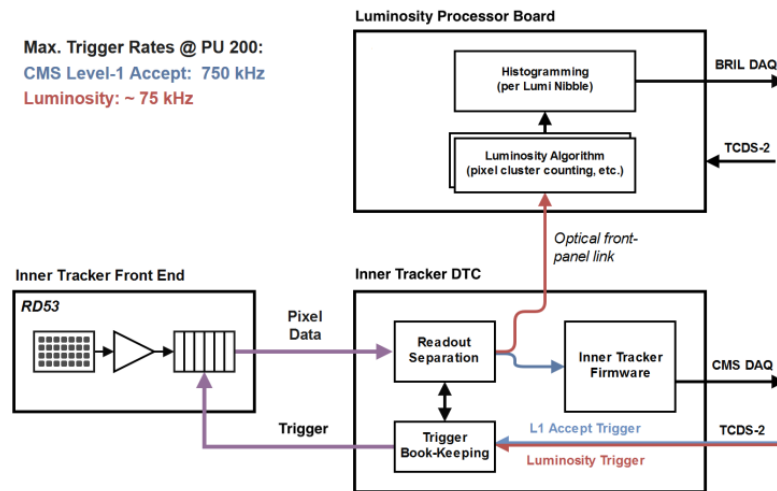
## 2. LUMINOSITY MEASUREMENT USING TEPX & D4R1

Luminosity measurement requires a detector (luminometer) that counts a quantity (e.g., rate of hits, clusters, coincidences) that is linear with the number of primary interactions. Luminosity measurement during Phase II [2] will be done using various CMS subsystems [1], including the full TEPX and its independently operated D4R1 ring. TEPX will be used in physics conditions for tracking but will also receive dedicated luminosity triggers generated by the BRIL Trigger Board (BTB). The TEPX data will be sent to a luminosity processing board and then to the data acquisition (DAQ) system BRILDAQ [3] which is independent of CMS central DAQ.

TEPX and D4R1 will be driven by the BTB in order to have full control over luminosity triggers. Measurement of beam induced background using D4R1 during the LHC ramp will need to be independent of the CMS clock. D4R1 will receive a dedicated control stream from the BTB that is based on the LHC clock and will be fully independent of the CMS Timing and Control

Distribution System 2 (TCDS2) and DAQ systems [4] [5]. TEPX luminosity data will be readout with a trigger rate of 75 kHz (an additional 10% of the L1 trigger rate) at  $\langle \text{PU} \rangle = 200$ . D4R1 will use the full readout capability of 825 kHz. During van der Meer scans ( $\langle \text{PU} \rangle = 0.5$ ), TEPX will be readout at 1 MHz trigger rate and D4R1 at 2 MHz (possibly higher).

Data accepted by the CMS L1 physics or luminosity triggers will be collected by the frontend pixel readout chip and sent through electrical links (eLinks) at 1.28 Gb/s to a low power GigaBit Transceiver (lpGBT) [2]. Optical links operating at 10 Gb/s will transfer the data from lpGBT to the backend Data Trigger Control (DTC) system. TEPX luminosity data will be separated and transferred to a special Luminosity Processor Board (Lumi Board) via 25 Gb/s optical links as shown in Fig. 2.



**Figure 2:** Data flow for CMS Phase II Inner Tracker used for luminosity measurement [2] [3].

### 3. TEPX CLUSTERING ALGORITHM

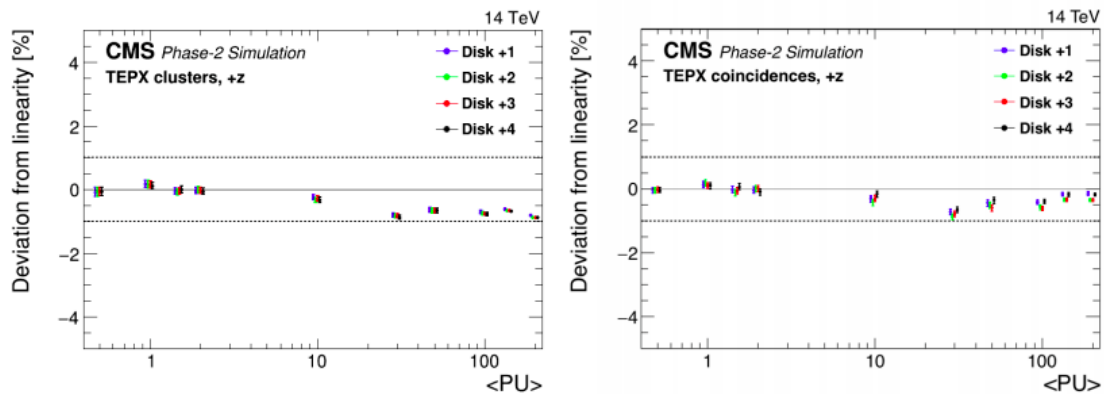
Luminosity measurement using TEPX will be based on real-time pixel cluster counting (PCC) per chip, implemented on FPGA. The algorithm counts the number of clusters, reconstructed from neighbouring pixels with charge deposit (hits), per LumiWord (approximately 1 s integration period) bunch-by-bunch in Zero Bias events. Due to the overlap in  $r$ - $\phi$  of the modules, two-fold coincidences of clusters [6] can also be counted for modules in the front and back layers of a TEPX disk. Two-fold coincidences in  $\phi$  arise from module overlap within the same ring and coincidences in  $r$  arise from module overlap between adjacent rings of the same TEPX disk.

TEPX luminosity data processing will be done per chip using FPGAs on the Lumi Board which will host clustering and histogramming instances. The clustering firmware will include the stream decoder that will receive TEPX chip data. The quarter core processor will identify up to four possible clusters within one quarter of a chip. Two hits belong to the same cluster if they touch horizontally, vertically or diagonally. The quarter core distributor will check the borders of a given quarter core for isolation and decide whether it has to be sent to the row and column merger or directly to the count accumulator. The count accumulator will receive the final cluster data and increment the cluster count.

A prototype pixel cluster counting algorithm has already been developed on FPGA and tested by injecting official CMS software (CMSSW) simulated TEPX events at an average 1 MHz event rate. The maximum trigger rate at  $\langle \text{PU} \rangle = 200$  was determined to be  $1.33 \pm 0.44$  MHz based on the simulation of the detector occupancy, which satisfies the D4R1 requirements.

#### 4. TEPX & D4R1 EXPECTED PERFORMANCE

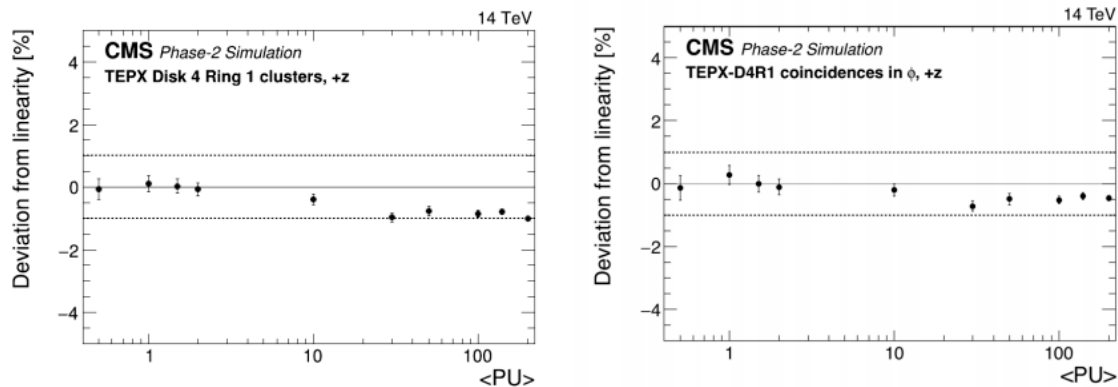
Simulated data samples for Phase II were produced using CMSSW including full CMS detector simulation implemented in GEANT4 [7]. The samples contain single-neutrino events overlaid with a variable number of minimum-bias events (events with at least a minimal amount of activity observed in CMS) to simulate different pileup values. Linearity for TEPX and D4R1 luminometer is expected to be within 1% over entire pileup range as shown in Fig. 3 and Fig. 4. The expected statistical precision of counting rate over 1 s integration time period for TEPX and D4R1 luminometers under high pileup conditions is around 0.1%.



**Figure 3:** Residuals of the mean number of clusters and coincidences with respect to linear behaviour extrapolated from a fit at low pileup values for each TEPX disk as a function of pileup based on CMSSW simulation [2].

#### 5. BEAM INDUCED BACKGROUND MEASUREMENT USING D4R1

D4R1 will have dual purpose, luminosity and beam induced background (BIB, including beam gas & beam halo) measurements. It will be operated from the LHC ramping phase (when beams are accelerated) to monitor BIB rates using the first bunches of trains or non-colliding bunches. Based on Run 2 experience, BIB is only expected to dominate over out-of-time contributions (primarily afterglow) after at least 30 empty bunch crossings ( $\approx 0.75 \mu\text{s}$ ). Incoming beam induced background will be separated from the first collision products by about 17.8 ns at the position of D4R1. The D4R1 readout timing will be fine-tuned so that the incoming beam induced background will be seen one 25 ns clock cycle before the collision products to be clearly distinguished from them. The timing optimisation for best efficiency is done by comparing CMSSW BIB simulations with physics collision simulations at high pileup to extract time of flight vs. deposited charge distribution for the two samples.



**Figure 4:** Residuals of the mean number of clusters and coincidences with respect to linear behaviour extrapolated from a fit at low pileup values for Disk 4 Ring 1 as a function of pileup based on CMSSW simulation [2].

## 6. Summary

The CMS detector will undergo several upgrades for the HL-LHC era. The Inner Tracker TEPX system will be used for tracking, luminosity and beam induced background measurements. Luminosity measurements by TEPX will be based on real-time pixel cluster or coincidence counting methods implemented on FPGA. Trigger and timing for luminosity measurement will be provided by the BRIL Trigger Board, allowing independent operation of D4R1 from central CMS TCDS2 and DAQ services. Luminosity processing will be performed by a separate Luminosity Processor Board hosting pixel cluster counting and histogramming firmware to which the IT-DTC backend will send the data. Beam induced background measurement will be done by D4R1 utilizing the first bunch in trains or non-colliding bunches. D4R1 will be operated on the LHC clock during LHC ramps. Linearity of the TEPX and D4R1 luminometers are expected to be within 1% (offline) up to a pileup of 200 and their statistical precision per second is about 0.1% at  $\langle \text{PU} \rangle = 200$ .

## References

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