

FELIX-based Data Acquisition System Integration with the NSW Micromegas Electronics and Detector Performance Validation

Christos Bakalis,^{a,b,*} Maria Perganti^a and Theodoros Alexopoulos^a

^a*National Technical University of Athens,
Athens, 15773, Greece*

^b*Brookhaven National Laboratory,
Upton NY 11973, USA*

E-mail: christos.bakalis@cern.ch

The foreseen upgrades of the Large Hadron Collider (LHC) are expected to increase the required throughput of the front-end and back-end electronics that support the readout of the LHC detectors. In some cases, new detector subsystems will have to be deployed, alongside next-generation data acquisition systems, both designed to cope with the luminosity increase. An example of this is the New Small Wheel (NSW) upgrade of the ATLAS detector [1]. The NSW will be comprised of two gaseous detector technologies, namely the Micromegas (MM), mainly used for track reconstruction, and the small strip Thin Gap Chambers (sTGC), mainly used for triggering. Prior to its integration with the sTGC wedges, each MM wedge is being fully-tested at the BB5 commissioning site. A series of tests are being run, from high-voltage stability to gas flow tests. But what will be studied in this work, are the application-specific tools that ensure proper flow of cosmic ray data, in order for them to be analyzed and confirm the detector's tracking capabilities before they are lowered into the ATLAS cavern.

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1. Front-End Link eXchange and the NSW Electronics

The keystone of the ATLAS Data Acquisition (DAQ) system will be the *Front-End Link eXchange* or simply *FELIX* [2]. FELIX will essentially be a bridge between the front-end electronics of all ATLAS detector subsystems, and their corresponding back-end components, which will mostly be software-based, whereas FELIX is an FPGA-based system housed by a commercial server. A configurable and flexible system, FELIX is essentially a data routing device, capable of mediating slow control, collision, and Trigger, Timing and Control (TTC) [3] information. Situated in the counting room, or Underground Service Area 15 (USA15), FELIX connects to the front-end electronics of the ATLAS cavern via optical links, or *GBT links*, each one of which is running at 4.8 Gb/s. For the NSW case, FELIX will interface with the front-end nodes over twenty-four optical links which are connected to the GigaBit Transceiver (GBTx) Application-Specific Integrated Circuit (ASIC) [4]. This radiation-tolerant chip is responsible for receiving the optical data from FELIX and serializing them over electrical links (hereinafter referred to as *E-links*) to various front-end nodes, while it also distributes reference clocking. On the opposite direction, the GBTx receives serial data from the aforementioned front-end nodes, before merging them into packets that are in turn transmitted back to FELIX via the GBT links. GBTx and FELIX is a standardized pair for high energy physics experiments with large throughput and bandwidth requirements, which are also conducted in a high radiation environment. For the NSW case, the GBTx is housed by the Level-1 Data Driver Card (L1DDC) [5], which is connected with eight front-end boards.

On the front-end side of the NSW electronics, three ASICs play the role of acquiring data, configuring, and monitoring. The VMM [6], digitizes the pulses formed by the detectors when muons traverse the chamber's medium. These digitized data are stored in its internal buffers, and can be queried and extracted upon the reception of a *Level-0* trigger signal. This signal is driven to the VMM by the Read-Out Controller (ROC), which also receives an 8b10b-encoded stream from the VMM, that contains the particle-related information. The ROC then forwards the data to the GBTx via dedicated E-links. The calibration, configuration and monitoring of both aforementioned chips is being conducted by the Slow Control Adapter (SCA) [7]. This chip receives the configuration data from a dedicated software suite [8] that interfaces with FELIX, and uses its peripheral interfaces (e.g. I²C) to parse them into the other front-end ASICs. It also features Analog-to-Digital Converters (ADCs) that are used to calibrate the VMM, and monitor the on-board temperature. For the Micromegas detector case, these chips are integrated in the Micromegas Front-End Board (MMFE8), which deploys eight VMMs, one ROC, and one SCA. A reduced version of the system can be examined in Figure 1.

2. The Micromegas Commissioning Site and its DAQ Needs

Prior to the deployment of a Micromegas detector wedge in the ATLAS cavern, several tests need to be run in order to validate its performance. These are conducted in the BB5 commissioning site at CERN, where the chamber is fully instrumented with 128 MMFE8s and 16 L1DDCs. To emulate the final DAQ system, these are read-out FELIX, which is also used to configure the front-end ASICs, and distribute trigger signals which originate from scintillators, stimulated by cosmic

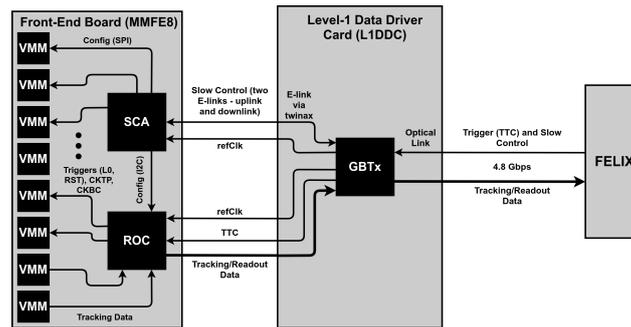


Figure 1: Breakdown of the Micromegas electronics data paths. In this figure, only one of the sixteen bidirectional FELIX optical links, and only one of the eight GBTx serial E-links are depicted. I.e. there are eight MMFE8s connected with each L1DDC, and sixteen L1DDCs connected to one FELIX instance.

muons that also traverse the detector medium. The final goal is to acquire enough cosmic data to ensure that the detector’s functionality is sound, in a narrow time-frame (about two weeks per wedge), to meet the stringent project requirements, both in terms of turnaround time, and actual detector and electronics performance. A photograph of the experimental setup can be examined in Figure 2.

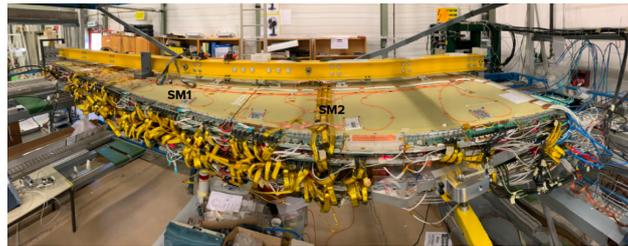


Figure 2: Photograph of a Micromegas sector while on the BB5 cosmic stand. Highlighted are the SM1 and SM2 parts of the detector (conceptually and structurally broken in two parts). One can also see the front-end electronics mounted on the detector, and the cabling connecting them. Four scintillators are not visible here, but are situated on top of the detector.

Software tools were developed that ensure the data transfer between the GBTx and the ROC is error-free. On one direction, the trigger (or TTC) information is transmitted by the GBTx to the ROC via an E-link running at 320 Mb/s. These data are encoded in an eight-bit word which yields eight possible commands (e.g. soft-reset, Level-0 trigger). Clock phase misalignment may lead to bit misinterpretation, which can cause the DAQ system to fail. Therefore, an automated procedure had to be devised, that would ensure that the ROC’s clocking settings are optimal. This procedure is conducted by a set of scripts which form the *Netio Traffic Analyzer* package [9]. Upon installation of a sector on the BB5 cosmic stand, the analyzer is used for validation of the data paths via test-pulsing. The TTC path evaluation is performed by evaluating the ROC’s performance while issuing test pulses to its associated VMMs. The main routine of the package is implemented in an `expect` script¹, that configures the front-end electronics of the sector-under-test by following a fail-safe sequence, issues test-pulses to the VMMs via a dedicated module connected to FELIX,

¹A subset of the TCL scripting language.

and records the data output of the ROCs in a round-robin manner, using the back-end NetIO [10] interface of FELIX. Also, this method validates the E-links that carry the muon data from the ROC to the GBTx. Data corruption on these E-links (which also mostly operate at 320 Mb/s) would result in malformed packets, that can be detected by the software package. These usually point to erroneous GBTx configuration or hardware failure, since the GBTx features an automated logic that aligns its deserializing clock with the inbound data stream.

Apart from validating the data transfer between the front-end electronics and FELIX, another aspect of this work is a hardware add-on that assists the detector's cosmic muon validation procedure. As mentioned above, scintillator trigger signals originate from muons that also go through the detector. These events are asynchronous to the reference clock of the DAQ system. This is not true for the ATLAS' case however, since the muons that originate from the interaction point are synchronous to the reference clock (or bunch-crossing clock). This is very useful for angled track reconstruction, as the timing is well-defined. In order to emulate this scenario, a Xilinx[®] board was deployed, conceptually situated between the scintillators and FELIX. The Field-Programmable Gate Array (FPGA) of that board, houses a firmware codebase [11], that performs the so-called fine-trigger selection. The device accepts raw scintillator trigger input, and compares it to the system clock. If a trigger signal's rising-edge coincides with the rising-edge of the reference clock (with 1.5625 ns accuracy), it is forwarded to FELIX, and consequently to the boards. If it is not, it is discarded. This of course reduces the readout rate (by about 90 %), but it emulates the event-trigger synchronization of ATLAS, thus providing another testing aspect of the detector's tracking capabilities, prior to its installation. The scheme can be examined in Figure 3.

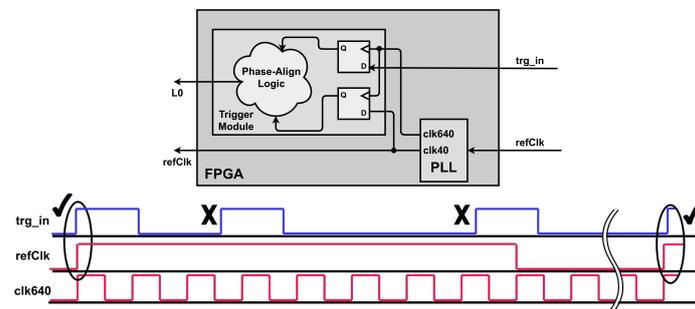


Figure 3: Top: Block diagram of the fine triggering logic. The FPGA's *Trigger Module* accepts the trigger from the scintillator, alongside the reference clock. The Phase-Align logic (clocked at 640 MHz), registers both the trigger and the reference clock, and determines if their rising edges coincide. If they do, a trigger is forwarded to FELIX (denoted as *L0*). Bottom: Timing diagram depicting the behavior of the Phase-Align logic. The encircled and checkmarked input triggers will be forwarded to the front-ends as an *L0* signal, thus initiating readout.

Acknowledgments

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References

- [1] ATLAS Collaboration - *Technical Design Report - New Small Wheel*. CERN-LHCC-2013-006, ATLAS-TDR-020, <https://cds.cern.ch/record/1552862>.
- [2] J. Anderson et al. - *FELIX: The New Approach for Interfacing to Front-End Electronics for the ATLAS Experiment*. Journal of Instrumentation, Volume 11, 2016, DOI: 10.1109/RTC.2016.7543142.
- [3] S. Ask et al. - *The ATLAS Central Level-1 Trigger Logic and TTC System*. Journal of Instrumentation, Volume 3, 2008, DOI: 10.1088/1748-0221/3/08/p08002.
- [4] P. Moreira et al. - *The GBT Project*. Proceedings of the Topical Workshop on Electronics for Particle Physics, 2009 DOI: 10.5170/CERN-2009-006.342.
- [5] P. Gkoutoumis - *Design and development of the Level-1 Data Driver Card (LIDDC) for the New Small Wheel upgrade of the ATLAS experiment at CERN*. Natl. Tech. U., Athens, Thesis, 2019, CERN-THESIS-2019-039 <https://cds.cern.ch/record/2674048>.
- [6] G. De Geronimo et al. - *VMM1 - An ASIC for Micropattern Detectors*. IEEE Transactions on Nuclear Science 60 (3) (2013) 2314-2321, DOI: 10.1109/TNS.2013.2258683
- [7] A. Caratelli et al. - *The GBT-SCA, a Radiation Tolerant ASIC for Detector Control and Monitoring Applications in HEP Experiments*. Journal of Instrumentation, Volume 10, March 2015, DOI: 10.1088/1748-0221/10/03/C03034.
- [8] P. Moschovakos et al. - *A Software Suite for the Radiation Tolerant Giga-bit Transceiver - Slow Control Adapter*. 17th Int. Conf. on Accelerator and Large Experimental Physics Control Systems, 2019
- [9] *NetIO Traffic Analyzer Software Repository*.
https://gitlab.cern.ch/cbakalis/netio_traffic_analyzer
- [10] J. Schumacher et al. - *High-throughput and low-latency network communication with NetIO*. ATL-DAQ-PROC-2017-010, <http://cds.cern.ch/record/2260396>.
- [11] *VMM Readout System Supervisory Board FPGA Firmware Repository*.
https://gitlab.cern.ch/cbakalis/vsb_daq