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An Advanced Triggerless Data Acquisition System for the GRAPES-3 Muon Detector

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The large area (560 m^2) muon telescope at Gamma Ray Astronomy at PeV Energies phase -3 (GRAPES-3) experiment in Ooty, India was designed primarily to study extensive air showers (EAS) and made operational in the year 1998. It has turned out to be a unique instrument capable of studying exotic phenomena by introduction of a new parallel data acquisition system (DAQ) in year 2000 to measure the muon directional flux. The recent discoveries of transient weakening of Earth's magnetic shield probed by a Cosmic Ray Burst [1] and measurement of the electrical properties of a thundercloud through muon imaging [2] has demonstrated the capabilities of this instrument. The design and deployment of a new triggerless muon data acquisition system (TM-DAQ) using Field Programmable Gate Array (FPGA) would enhance the present capabilities and open a new window on several physics fronts such as, a) precise measurement of the muon flux for thunderstorm studies, b) study of large angle EAS using the muon component, c) search for exotic particles characterized by early or delayed arrivals. We present here the salient features of the TM-DAQ along with initial observations.

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1. Introduction

The GRAPES-3 experiment is operating with 400 numbers of plastic scintillator detectors spread over an area of 25000 m^2 and 3712 proportional counters (PRCs) covering an effective area of 560 m^2. Here a PRC is a sealed gas-filled type detector made by using a $600 \times 10 \times 10\,cm^3$ mild steel hollow tube which is filled with P10 gas, a mixture of Argon (90%) and Methane (10%) above local atmospheric pressure by employing a brass needle valve on the back-plate. A 100 μm thick tungsten wire is used as the anode of the detector which is strung across the length of the detector with help of pair of glass-Kovar hermetic seals at both the ends. Figure 1(a) shows the schematic representation of a PRC. The detector operates in pulse mode and the pulse amplitude provides the information on the number of particles. The analog pulse from the detector with a decay constant adjusted to 7 us is connected to an amplifier with a gain ratio of 83. Each PRC has its dedicated amplifier and the amplified output is connected to a discriminator with a threshold value adjusted to -100 mV, the varying width output from a discriminator is proportional to the logarithm of the PRC pulse amplitude. The tracking capabilities for the muon telescope are obtained by the placement of PRCs in 4 layers with 58 PRCs in each layer and every alternate layer is placed orthogonal to each other, two layers of PRCs are separated by 15 cm thick concrete blocks, providing a mean angular resolution of 4°. A concrete absorber of 2 m thickness in inverted pyramid shape above the top layer of PRC's provides a 1 GeV threshold for the vertical muons as shown in Figure 1(b). A total of 232 PRCs placed in 4 layers as per the above-mentioned layout is called a muon module.

The initial DAQ for PRC [3] was designed to make observations only with respect to the EAS trigger, which is generated by an array of plastic scintillator detectors [4]. The block diagram of the existing system is shown in Figure 2(a), where all the digital outputs from the discriminator corresponding to 58 PRCs from each layer of a module are brought to the digital wave memory card and stored in the cyclic memory for a duration of 85us. On the arrival of an EAS trigger the writing to the memory is stopped and read operation is performed from all 4 digital wave memory

(DWM) card. Using DWM control card the arrival time of muons with respect to EAS trigger with resolution of 167 ns and pulse width with a resolution of 300 ns for all the hit counters are transferred to EAS muon data card which interfaces the data to the computer (PC1). The logical OR of all 58 PRCs output in a layer called layer-OR and coincidences of layer-OR signals like 2-fold, 3-fold, and 4-fold are monitored using monitor data card in multiplex mode.

An additional DAQ was designed and installed in the year 2000 as shown by dotted lines in Figure 2(a) to record the directional flux of muons using an independent self trigger generated by each muon module called a four fold trigger (4F-trigger). As shown in Figure 1(b) when a muon passes through all the four layers of a module and hitting at least one PRC in each layer a coincidence 4F-trigger at the rate of ~3.2 kHz is generated by the module. The status of each PRC is latched in pulse latch cards on the arrival of a 4F-trigger and stored in the large memory bank available on the module control card. The data from all the four modules of a super-module is read every second via a common control card and transferred to the computer (PC2) via a PCI interface card. Since the trigger rate is very high and data volume becomes 1.5 GB / hour per super-module, totaling to 144 GB per day for all super-modules which was very large considering the available technology for storage devices during year 2000. Thus to overcome that the DAQ system makes a histogram for arrival directions every 10 s and stores them for further analysis which results in data volume of 4GB per day for all super-modules. The existing system which was designed two decades back is working fine as desired, but it imposes challenges in terms of maintenance where all components are getting obsolete and the interfaces used are outdated. Additionally, the current system functionality can be further enhanced by improving on parameters like dead time, which is 15-20% presently. The dead time is directly proportional to EAS trigger rate (~45 Hz), and considering the future expansion of the plastic scintillator array, the expected EAS trigger rate will increase to ~100 Hz. The dead time for existing muon DAQ would become very large and unacceptable.

Using an embedded system design approach a FPGA based compact, powerful and programmable TM-DAQ was designed, it overcomes all the bottlenecks of the existing system, and provides finer resolution of data with complete flexibility to collate data between all modules. The Figure 2(b) shows the block diagram of the new DAQ which utilizes essentially 2 numbers of FPGA based cards where each one can interface with 158 independent PRCs. One of them is configured as master and the other as a slave card, hardware for both of them are same and basic functionalities are similar however, the master has an additional interface to communicate with PC via USB and in future using TCP/IP protocol, the master card is also responsible for communication between slave card to PC using SPI protocol the detail description of the functionality is covered in next section.

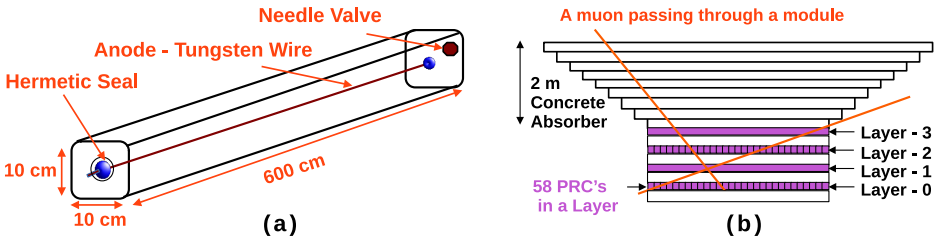

Figure 1: Schematic view of (a) A PRC and (b) PRC's placement in a muon module

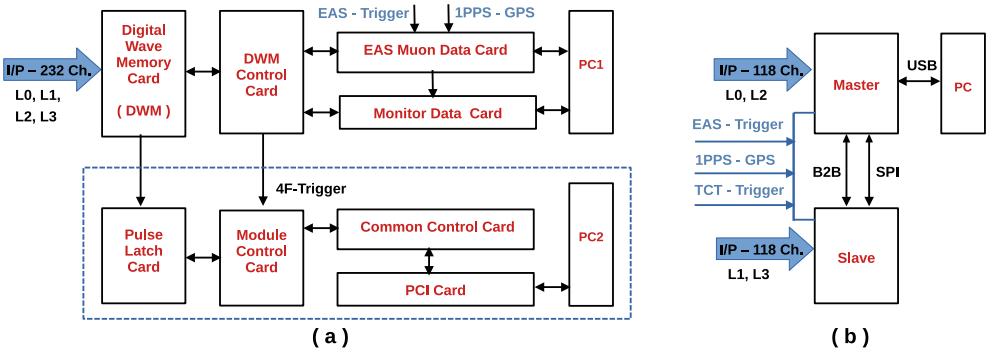

Figure 2: Block diagram representing DAQ for a muon module (a) existing and (b) new

For sharing the layer-OR signals between the two cards board-to-board (B2B) communication is established using flat ribbon cable.

2. Hardware for Triggerless Muon Data Acquisition System

The core component used for the design of GRAPES-3 TM-DAQ is a compact powerful board designed by ALICE collaboration for its detector at LHC Point 2, CERN Geneva during Run I phase of LHC. The board is a High-Level-Trigger (HLT) Read-Out Receiver Card (H-RORC) [5], henceforth called as ALICE board. In total 140 ALICE boards were gifted by the HLT group of ALICE collaboration during the ALICE upgrade after Run 1 data collection. We have designed an interface card that provides the interconnection between ALICE board and the GRAPES-3 system and developed the firmware for its use as TM-DAQ.

An ALICE board is a ten layer compact printed circuit board (PCB) compatible to fit in the PCI slot of a computer. It has a XILINX make Virtex4 XC4VLX40 [6] FPGA as a powerful device for all digital logic processing, supported by 4 numbers of DDR SDRAM, a high-speed dynamic random-access memory of capacity 256 Mbits each with fast access time and high-speed data rate of 400 Mbps [7]. Two numbers of onboard crystal for generating clock of 100 MHz and 50 MHz to be used as the system clock and user clock respectively with frequency stability of 50 ppm. A PHY chip for TCP/IP and TAGNET connectors with differential I/O's are available. For programming, debugging and boundary-scan testing using IEEE standard JTAG interface is also available onboard. The board was meant to be used in PCI slots of a computer, but the provision is available to take power either from PCI or an external 3.3 Volts DC supply. A total of 158 user accessible I/O pins are available on tyco connectors.

The placement of PRC detectors is modular as explained in the previous section where each of the 16 existing modules consists of 232 PRCs per module, and we are in process of expansion of muon detectors by installing 16 additional modules which will have 236 PRCs per module. Thus we have made a provision of 236 input channels for the new DAQ which would cater to both the new and old modules without any hardware changes. Considering the logical resources of FPGA and available I/O's on tyco connectors, we have estimated that single ALICE board will be sufficient for 118 PRC channels. Thus, we adopted design topology based on the concept of master and

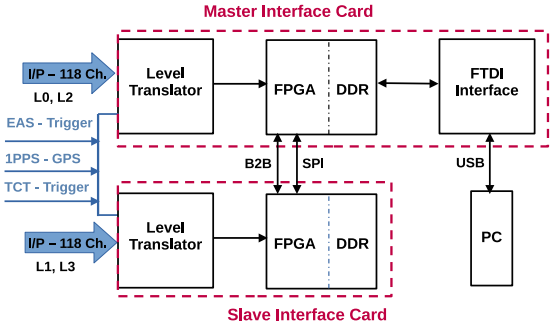

Figure 3: Block diagram of hardware for TM-DAQ

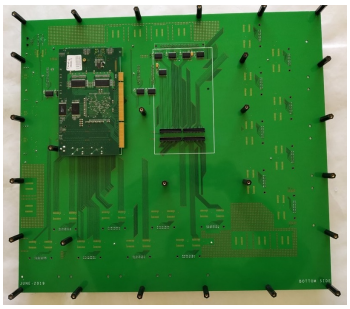

Figure 4: Picture of ALICE board mounted on interface card

slave, where both cards handle the inputs from 118 independent channels and the master card takes additional role for transfer of data both from master and slave card to PC, a block diagram for the above topology is shown in Figure 3. The output from the front-end electronics discriminator card is a TTL standard signal with varying width, available on a 16-pin FRC connector for 8 channels, whereas the specified input for the ALICE board is an LVTTL standard and the interface for I/O pin are available on a tyco connectors. Thus as a first step, an interface card was designed to house non-inverting transceiver buffer SN74LVC245A [8] which is configured to provide an LVTTL signal compatible to the input of ALICE board. The board has connectors that matches with discriminator output and ALICE board inputs. The ALICE board sits on the interface card and forms an integral unit. A picture of an ALICE board mounted on an interface card is shown in Figure 4. The provision for communication between the master-slave cards and receiving of other external triggers like EAS-trigger, TCT-trigger, and 1PPS-GPS has also been provided on the interface card.

3. Firmware for Triggerless Muon Data Acquisition System

The complete firmware has been developed by using hardware description language (HDL) Verilog, and a functional block diagram of all the firmware modules embedded in the FPGA is shown in Figure 5, the concept of state machine has been the core of our design approach in each module, thus making the firmware robust. The bidirectional communication between the PC and the ALICE board is established using an FT2232H [9] over USB 2.0. The initialization process begins with clearing of all the registers in the hardware and control word exchange (CWE) between hardware and PC. A success prompts the loading of GPS time into the real-time clock (RTC) module of both master-slave cards. After a successful handshake between master card to slave card and validation of the loaded parameters the data acquisition process begins. The very first block in the firmware module is the signal validation module (SVM), all the signal inputs to the cards are passed via SVM where any spurious noise signal of width less than 200 ns would be blocked and does not propagate to the next stage for processing. After qualifying the SVM the varying width output from the discriminator described in section 1 are sent to the pulse width and timing (PWT) module and trigger (TRIG) logic module which are described in a later section. The PC side code has been developed using C language and for all data communication between the hardware and PC

via USB using FTDI module, a cyclic redundancy check (CRC) at application level is generated to maintain the data integrity.

3.1 Pulse Width and Timing (PWT) and Trigger Logic Module

The PWT module makes measurement of pulse width (pw) from all the signals simultaneously with a resolution of 10 ns and latches the arrival time (ta) of each individual pulses with a resolution of 10 ns. The 16-bit wide pulse width information padded with layer and channel ID along with 32 bits of arrival time is temporarily stored in onboard DDR which is later transferred to PC via FTDI. Figure 6 shows a typical amplified PRC signal along with its discriminator output pulse. The PWT measurement is also performed for EAS-trigger, TCT-trigger, and 1PPS signal from GPS unit, and two of the fold signals generated onboard namely 3-fold and 4-fold. The precision measurement of arrival time and width from all individual pulses simultaneously without any dead time makes the instrument versatile. However, the volume of the data generated is large ~2 Mbits / board / s, the availability of large DDR memory is utilized by configuring 2 numbers of DDR to operate in ping-pong mode. One of the memory DDR1 is in write mode where all the PWT data is continuously written and at the end of the 1 second time period the monitoring data is also written and status is changed to read mode and other memory DDR2 turns to write mode. The data stored in the DDR1 is read via an FTDI module and stored on a computer (PC).

The trigger logic module makes a logical OR for all the valid inputs from PRCs in a given layer and the output signal is called a layer-OR signal. Each card has inputs from 2 layers of a module thus 2 numbers of layer-OR are generated onboard, via an FRC interconnect cable (B2B) the layer OR signals are shared between master and slave card, thus at any given time the layer-OR from all the four layers are available in a card and after reshaping the layer-OR signal to a width of 3 μs, a coincidence for all combinations of 2-fold, 3-fold and 4-fold are generated.

3.2 Monitoring

The count rate mon (CRM) module has been designed to monitor detector performance parameters and critical hardware performance parameters. The individual hit rate from 118 PRCs connected to the card, logical combinations generated on board like layer-OR, 2-fold, 3-fold, 4-fold along with 1PPS, EAS-trigger, TCT-trigger are measured in CRM module and stored at end of each second into DDR. There are 3 numbers of temperature sensors on master-slave cards 2 of them are placed on top of onboard crystals of 100 MHz and 50 MHz, the third one is mounted on an

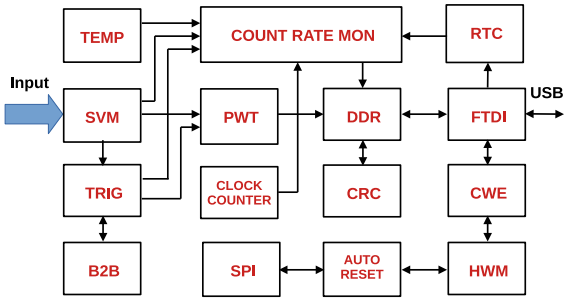

Figure 5: Firmware embedded in FPGA for TM-DAQ

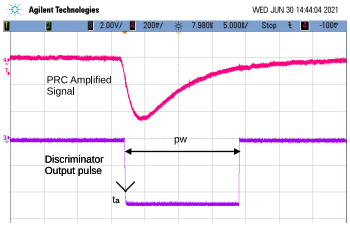

Figure 6: A typical amplified PRC signal along with its discriminator output pulse

interface card to monitor the room temperature. The temperature sensor output is processed by temperature module (TEMP) of the firmware and the measurements are stored in CRM module every second. Similarly, another firmware module clock counter makes a measurement on the numbers of pulses from 100 MHz and 50 MHz every second and records them in CRM module. Continuous monitoring of clock frequency and temperature of the crystals provides a very good handle to make corrections of clock drift due to changes in the temperature.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
HW	CWE	DDR3	DDR2	DDR1	T3	T2	T1	TCT	EAS	FTDI	WR	RXF	TXE	1PPS	IM

Figure 7: An 16 bit word for hardware parameter monitoring

The hardware monitoring module (HWM) is designed to monitor the status of various parameters of the FPGA, DDR memories, connected signals, and FPGA firmware status during its execution. As shown in Figure 7 a 16-bit word consisting of status from various modules will be logged in the DAQ computer along with CRM data and this features provides an in-depth continuous monitoring of hardware status and debugging in case of any issues. The initialisation monitoring (IM) monitors the status of the initialisation of all firmware modules and DDR memories. The complete communication cycle between the master card and PC is analysed by checking the status of FTDI control signals RXF, TXE, and WR. If any improper status in any of the above three bits is observed, an FTDI status bit would be flagged which would initiate the action of auto-reset.The input frequency range for the external signals 1PPS GPS signal, EAS-trigger, and TCT-trigger and operating temperature range is being monitored continuously and in case of any abnormality, the corresponding error status bit would be set. The status of the DDR memory chips DDR1, DDR2, DDR3, and their firmware module is stored in B11, B12, B13. The status of the Control Word Exchange (CWE) module is assigned to B14, at the start of the DAQ run, the USB communication from computer to FPGA via FTDI module is verified by this module. it indicates that the USB data read-write operations are working fine and the DAQ run can be started. Any wrong control word or no control word indicates a problem with the USB link and the status bit is set and an auto-reset operation is initiated in FPGA firmware as well as by the computer program to retry for operation. The last bit of the word B15 is generated by a logical condition, looking at the critical HWM parameters, if this bit is set it indicates a critical hardware (HW) error status.

4. Observations

The performance of the TM-DAQ was studied by installing the system for 4 numbers of muon modules in parallel to the existing DAQ, in Figure 8 the muon flux as measured by both the DAQs using 4F-trigger for a period of week during 24-30 June 2021 from one of the module are shown. The measured flux from the new DAQ (b) is larger by ∼20% as compare to the existing DAQ (a) which is a significant improvement. In existing DAQ the pulse width spectrum (PWS) of each PRC is performed in a multiplex mode thus it can monitor the performance of the PRC only for duty cycle of 1.5% however, the topology of new DAQ allows continuous PWS for each PRC, the Figure 9 shows a typical PWS with a prominent single muon peak ∼20 keV due to cosmic ray muons and self calibrating Fe and Zn peak at 6.4 keV and 8.6 keV respectively due to Kα X-ray emission,

with a resolution of 10 ns. It is now possible to study the EAS at large angles through the muon component using the software tool developed by our team and detail observations are presented by B. Hariharan et al. [10].

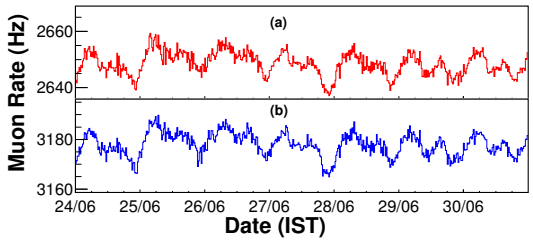

Figure 8: Muon flux measured using 4F-trigger (a) existing DAQ and (b) TM-DAQ

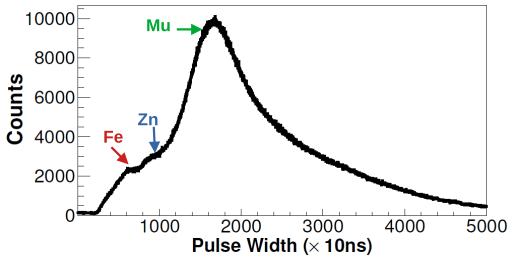

Figure 9: Pulse width spectrum observed for one of the PRC using TM-DAQ

5. Conclusions

The TM-DAQ concept with measurement of arrival time and pulse width for each PRC output with a resolution of 10 ns and implementation of TCT allows collating the data effectively among various modules and independent DAQ system which opens up the various new possibilities to look for the precision study of the muon flux during thunderstorm studies which happens at the time-scale of ms. Onboard temperature sensors allow to correct the clock drift (~20 Hz/°C) for precise measurement of arrival times.

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