

Improving Radio Frequency Detectors using High Performance Programmable Logic

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An increasing number of experiments are targeting GHz bandwidth impulsive radiation induced by high energy neutrinos in ice or high energy cosmic ray air showers. Beamforming triggers improve detection prospects as effective signal-to-noise ratio scales as the square root of the number of phased array antennas in a coherent sum. However, this also brings high technological requirements with an increasing number of narrower beams required, while sub-nanosecond synchronisation must be maintained across the antennas summed in each beam. A prototype digital beamforming trigger is developed using Radio-frequency-system-on-a-chip (RFSoc), an adaptable radio platform leveraging the advantages of Field Programmable Gate Arrays (FPGAs). Findings are presented including cross channel alignment, trade-offs between resource usage and trigger efficiency and using programmable logic for flexible digital filtering capabilities.

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1. Introduction

1.1 Radio Detection of Cosmic Rays and Neutrinos

The VHF-UHF radio bands (~10-1000 MHz) are well suited to the detection of impulsive Cherenkov radiation generated by neutrino-induced electromagnetic showers in dense dielectric media through the Askaryan effect [1, 2]. Glacial ice in particular is highly transparent to radio frequencies less than 1GHz [3]. Geosynchrotron emissions due to cosmic ray and tau neutrino air shower cascades are also coherent in the radio spectrum [4].

A variety of recent and planned experiments leverage the above, including LOFAR [5], CO-DALEMA [6], the Square Kilometre Array [7], the Pierre Auger Observatory upgrade (AugerPrime) [8], and prototypes deployed for ARIANNA [9] and GRAND [10].

The NuPhase detector at ARA [11] uses coherent beamforming at the trigger level to achieve a reduced signal threshold. Such a phased array trigger is also part of the proposed IceCube-Gen2 [12], the Radio Neutrino Observatory [13] as well as RNO-Greenland [14] which is currently being installed. This is also leveraged for high-elevation detection of tau neutrinos with BEACON [15].

The Payload for Ultrahigh Energy Observations (PUEO) [16] will provide the concrete example for this study. Designed for world-leading sensitivity to neutrinos at energies above 1 EeV, PUEO will improve on the sensitivity of the ANITA [17] long-duration balloon payload with an interferometric phased array trigger across the 216 antennas of the main instrument. Beams will be formed from 8 vertically grouped antennas for the level 1 trigger. PUEO will provide a factor of 5 improvement

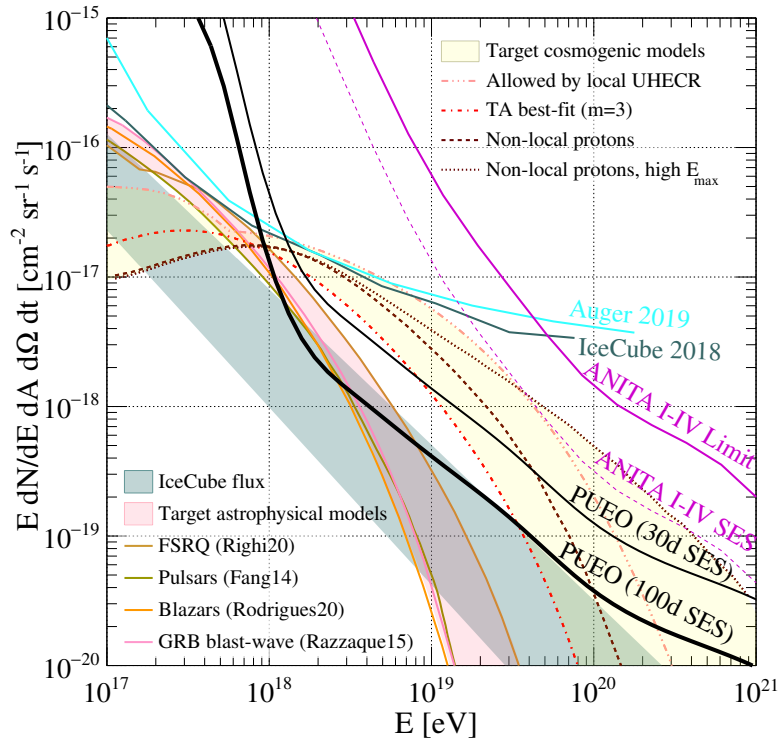


Figure 1: PUEO single event sensitivity to diffuse ultrahigh energy fluxes, compared to existing limits and cosmogenic/astrophysical models [16].

in the single antenna signal-to-noise ratio, translating to significant enhancement in sensitivity to ultrahigh energy neutrino fluxes (fig. 1).

1.2 Beamforming at Trigger

Coherent summing multiple channels relative to a signal lowers the signal energy threshold relative to thermal noise. With an N -antenna sum, uncorrelated thermal noise scale as \sqrt{N} , while a coherent signal add as N so that the signal-to-noise ratio (SNR) increases as \sqrt{N} .

Where data cannot be captured in full for later offline beamforming, this coherent sum requires "online" beamforming so it can be leveraged at the trigger level. The coherent sum must combine constituent antennas with time delays corresponding to the direction of the incident signals and configuration of the antennas. As a larger array of antennas are combined for each coherent sum, the width of the effective beams - where the sum is coherent and a high % of the SNR benefit is realised - is narrowed, increasing total number of beams needed. There is thus a high computational cost to trigger-level beamforming, posing a particular challenge when there is limited power availability, as is the case with PUEO.

1.3 Programmable Logic

Programmable logic such as Field Programmable Gate Arrays (FPGAs) provide a highly configurable platform naturally suited to bring the sensitivity improvements enabled by beamforming. Radio-frequency-systems-on-a-chip (RFSocS) [18] additionally combine FPGAs with analog-to-digital converters (ADCs) on the same chip, lower power consumption by reducing the size of the signal chain and integrating functionalities. A variety of commercial applications already use beamforming - including 5G communication and military radars - so that high performance multi-GHz RFSocS are commercially available at relative low cost (~€5000 at single unit pricing). A quantitative evaluation of their suitability for digital beamforming is presented, with a prototype implementation based on the PUEO requirements.

2. Beamforming prototype for PUEO using programmable logic

A prototype beamformer was developed for the ZCU111 RFSoc evaluation board [19] in the Xilinx development environment, with hardware block design and synthesis using Vivado Design Suite [20] and software developed in Xilinx SDK for clock programming by an on-board CPU. The antenna data is parallelised to 8 data samples per clock cycle, to enable the FPGA to meet timing requirements with 375 MHz clock. The DAC channels were used to simulate what would be received at the PUEO antennas, also generated by the CPU. Vivado's Integrated Logic Analyzer was used to capture the output of the beamforming threshold trigger. Figure 2a shows a schematic of the prototype trigger and the simulation environment. Figure 2b shows the beamforming improvement to the trigger threshold energy. Figure 3a compares the impact of the coherent sum window width on beamforming trigger efficiency for signals of two different widths.

2.1 Phase Alignment

The coherent sum requires the alignment of the signal across multiple channels. The geometry of the antennas determine the phase adjustments that must be applied to the input channels to achieve

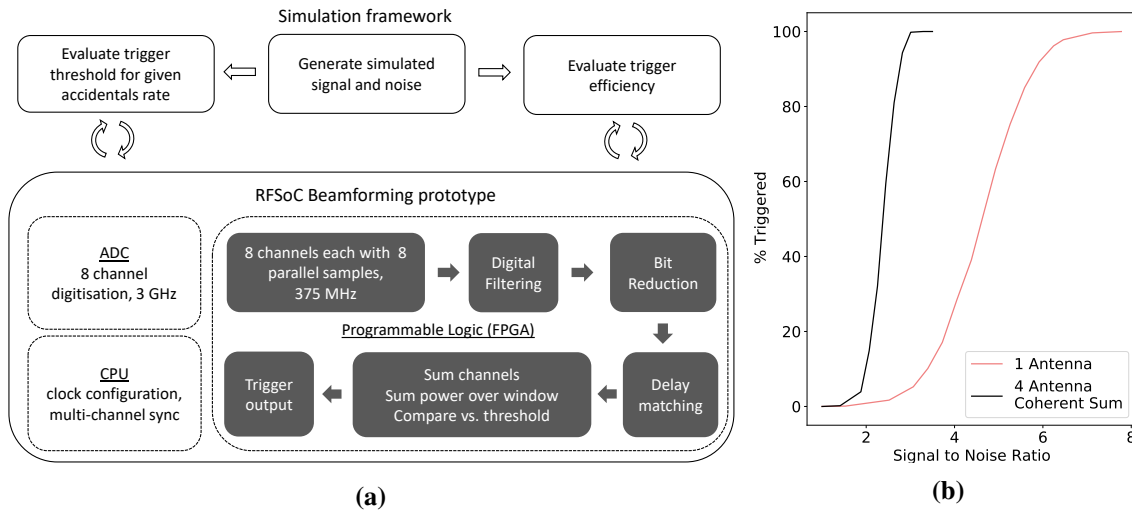


Figure 2: (a): Schematic for RFSoc beamforming prototype developed. (b): Reduction in trigger threshold demonstrated on the RFSoc beamforming prototype. A limitation of the XM500 breakout board providing access to the ADC channels means that the beamforming performance is only measured for up to 4 channels.

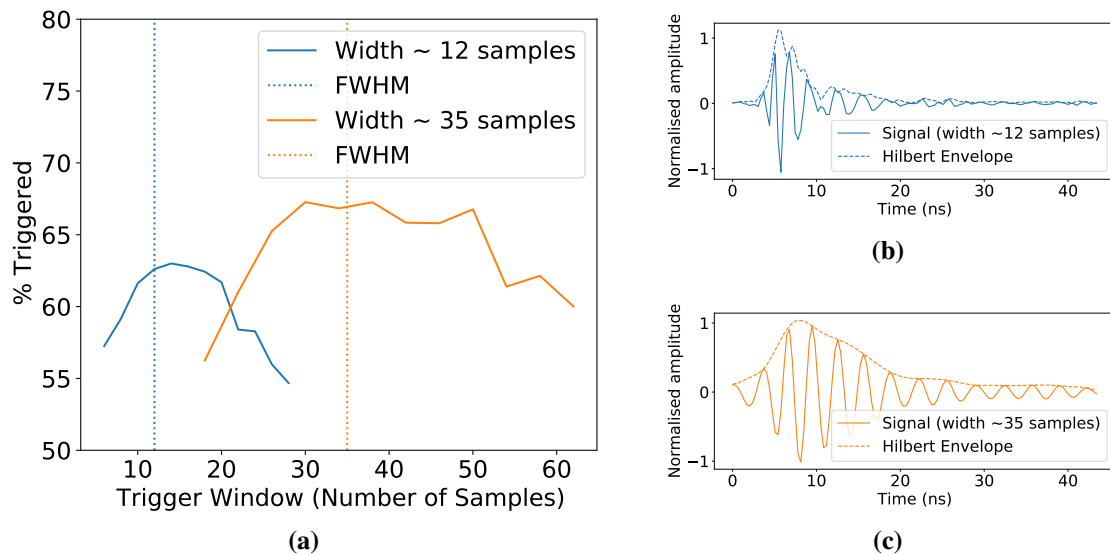


Figure 3: (a): Optimal size of the trigger window is dependent on the signal width, quantifiable by the full-width-at-half-maximum (FWMH) of its Hilbert envelope. Given a wide range of signal durations, there may not be a single optimal window size. (b, c): Signals with widths ~12 and ~35 samples

this alignment for a given source direction. The width of such a beam is then determined by the solid angle where additional phase mismatch does not reduce the SNR gain by more than some threshold. By considering this across the full field of view where the experiment is sensitive, an array of beams can be identified. For PUEO this is approximately 100 beams, across 2 polarisations, for each vertically arranged grouping of 8 pointed antennas. In addition to this geometric consideration for phase alignment, a predictable relationship is also required in the relative sampling phase between the ADC channels.

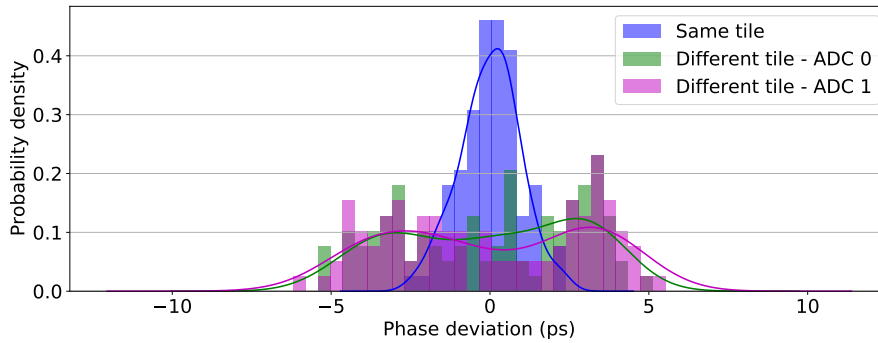


Figure 4: Phase variation across channels at 500 MHz, where each phase measurement is fitted over 5ns, comparable to the width of the optimal window for the threshold trigger.

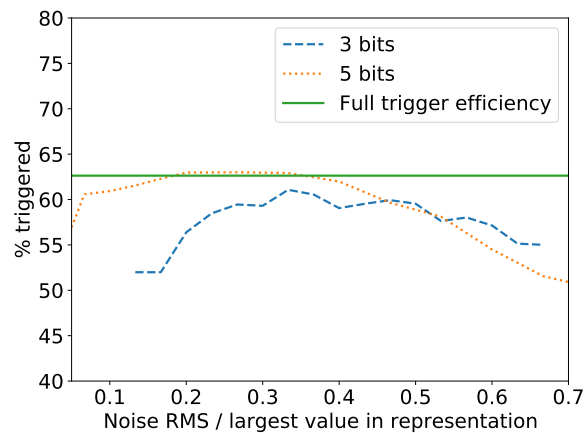


Figure 5: Trigger efficiency at SNR = 1.6. Keeping 5 bits retains maximum trigger performance as long as the noise RMS is kept within a specific range. 3 bits results in a small loss in fidelity even at optimal range.

Using externally generated sinusoids, fig. 4 shows the distribution of relative phase variation between channels on a single RFSoc. Broadband alignment across channels is also found to be within 10ps, which compared to the 333ps sampling period means the RFSoc introduces only negligible additional phase variation and does not affect the beamforming performance. No additional variation was found to be introduced when the RFSoc is power-cycled. It is noted that manufacturer-provided hardware and software examples did not enable cross-channel synchronisation and this is introduced through additional configuration of the clocking system.

3. FPGA Resource Constraints

Gen 1 RFSocs have 12-bit ADCs, offering high resolution digitisation for storage and digital filtering (see section 4). However, maintaining all 12 bits is not necessary for the beamforming trigger, and a reduction can reduce hardware resource requirements. During bit reduction, a particular value in the 12 bit representation can be mapped to 1 in the reduced representation, and the ratio between the two is used to scale all values. Values outside the max/min representable are clipped, and fractional values are rounded. Fig. 5 shows that reducing from 12 to 5 bits can

	DSP utilisation	CLB utilisation
12 bits	10%	25%
5 bits	5%	10%
3 bits	5%	6%

Table 1: Beamforming utilisation compared to resources available on the ZCU111 board.

retain full trigger efficiency, while 3 bits introduces a small loss of around 5% trigger efficiency. Reduced dynamic range means that the above are sensitive to the noise RMS level, which can be continuously measured and re-scaled.

Table 1 shows the utilisation for 100 beams, for the two main programming logic resources: Digital Signal Processing (DSP) slices and Configurable Logic Blocks (CLBs). Bit reduction significantly reduces resource utilisation for both. Note that these estimates include optimisations through carry-save, which efficiently add multiple numbers using fewer DSP operations.

4. Digital Filtering

As well as the core beamforming algorithm, the computational resources of the FPGA are well suited for additional digital filtering of antenna channels to increase coherent trigger performance. For PUEO the use cases include tunable notch filters for narrow band RF interference (RFI), which had caused particular issues for ANITA flights. The presence of RFI increases the trigger threshold of the beamformer and reduces detector sensitivity. Another application is to apply a band pass filter to increase the effective SNR, by suppressing frequency ranges where thermal noise is expected to dominate the signal in power.

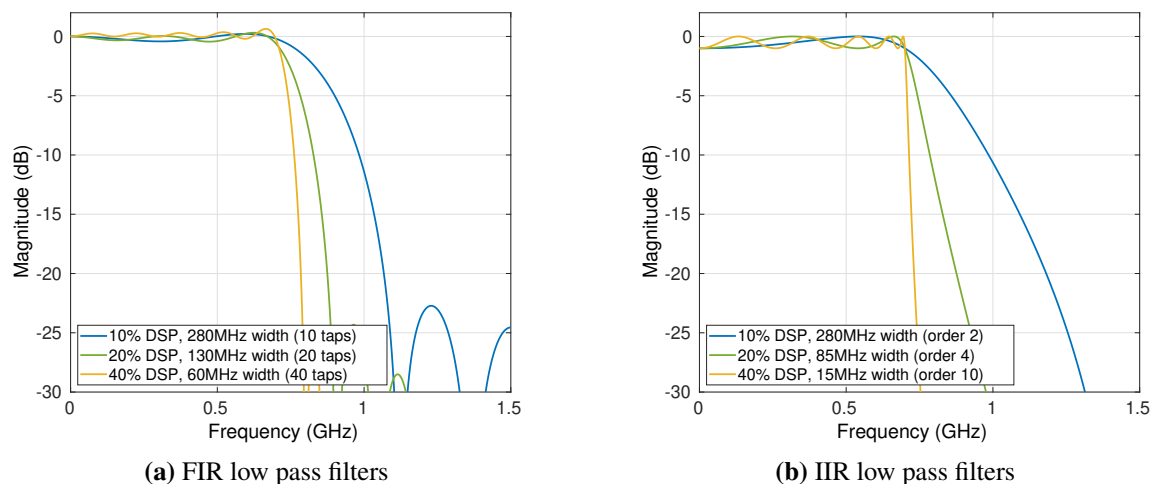


Figure 6: Comparison of low pass filter magnitude responses with pass frequency at 700 MHz, against resource usage on the evaluation board. If a steeply falling response is not required, FIR is preferred as it retains a linear phase relationship and therefore does not distort the signal. Bandwidths given to -10dB.

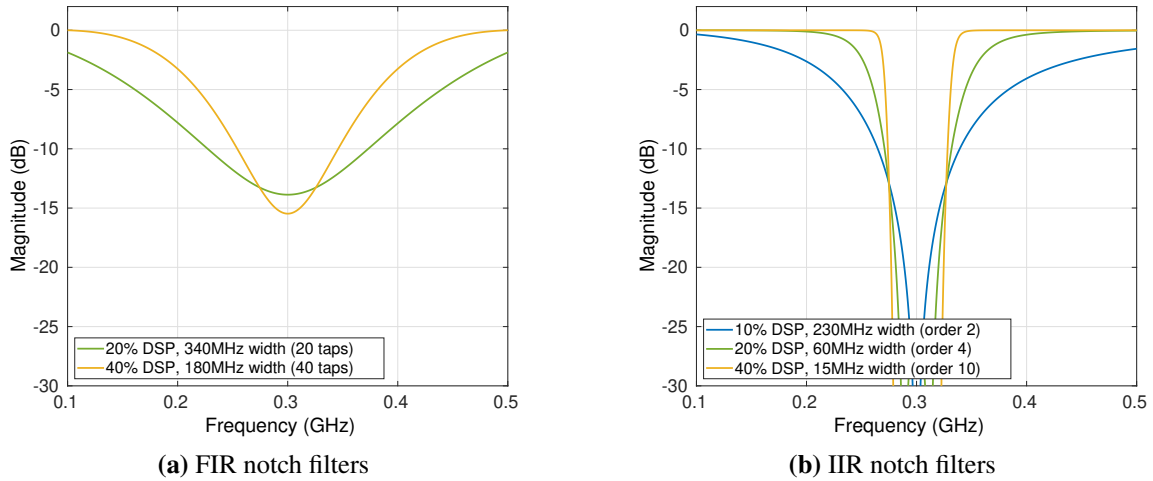


Figure 7: Comparison of notch filter magnitude responses, requiring a 50 MHz band with -13dB suppression at 300 MHz. As sharply falling notch filters enable more signal bandwidth to be retained, IIR filters may be best suited despite non-linear phase response and non-trivial implementation. Bandwidths given to -2dB.

Resource estimates from the previous sections show the majority of FPGA resource are still available after the core beamforming calculations. However, the requirement for multiple samples per clock cycle significantly increase the hardware resource cost of filter implementations. For Finite Impulse Response (FIR) filters, where there is no feedback, the number of multiplications (and thus DSPs required) scales linearly with the number of parallel samples. Infinite Impulse Response (IIR) filters are more difficult to scale due to the requirement for aligning feedback across both the sampling and clock rates, although several methods are available [21]. FIR filters are preferred where steeply dropping responses are not required, as they have linear phase response and preserve the shape of the signal. IIR filters are necessary for high-specification filters due to their relatively lower resource requirements. Figs. 6 and 7 compare the magnitude response and DSP utilisation for two example filters, without any optimisations (except symmetry of FIR coefficients) or additional complexity for IIR filters due to DSP latency.

5. Conclusion

Trigger level beamforming is a powerful technique for reducing energy threshold in the radio detection of high energy neutrinos and cosmic rays. Using the PUEO long duration balloon payload as an example, a prototype beamformer was developed on an RFSoc board which demonstrated the expected improvement in threshold signal-to-noise ratio and broadband phase alignment across channels. By reducing the number of bits fed into the coherent sum, the 100 beams required for the level 1 trigger of each group of 8 PUEO antennas can be reduced from 400 DSPs (10% RFSoc utilisation) to 200 (5% RFSoc utilisation). Remaining hardware resources can be leveraged for digital filtering capabilities, re-configurable in flight, although significant resources are required for their implementation due to multiple parallel samples for each FPGA clock cycle.

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