The HEPD-02 trigger and PMT readout system for the CSES-02 mission

Marco Mese,[a,b,*] **Giuseppe Osteria,**[b] **Valentina Scotti,**[a,b] **Antonio Anastasio,**[b]
Alfonso Boiano,[b] **Vincenzo Masone**[b] **and Antonio Vanzanella**[b] **on behalf of the
CSES-Limadou Collaboration**
(a complete list of authors can be found at the end of the proceedings)

[a] *University of Naples Federico II, Department of Physics,
via Cintia 21, Naples, Italy*

[b] *National Institute for Nuclear Physics (INFN),
via Cintia 21, Naples, Italy*

E-mail: marco.mese@unina.it

This contribution describes the Trigger board of the High-Energy Particle Detector, which will be placed onboard the second China Seismo-Electromagnetic Satellite for CSES-Limadou mission. This mission will monitor variations in ionospheric parameters that are supposed to be related to earthquakes. The first satellite is already in orbit and the second one will be launched in 2023.

The HEPD detector will be composed by a tracker made of CMOS sensors (ALPIDE sensors), followed by two segmented planes of plastic scintillators used for trigger signals generation.

The actual calorimeter will be composed by twelve planes of plastic scintillator and two segmented planes of an inorganic scintillator called LYSO.

The calorimeter is surrounded by five scintillator planes used as a veto system.

All the scintillators are coupled with PMTs, whose signals are acquired and digitized by the Trigger board, that also implements the trigger system for the whole apparatus.

The ongoing work on the Trigger board consists in the design of both the hardware and the firmware used for the communication with the other boards of the detector, power managing, and the interfacing with the ASIC used for PMTs' readout.

Eventually the Trigger board will be tested to verify its functionalities and its compliance with the HEPD design specifications. Next developments are the integration of the Trigger board with the other systems on the detector and the environmental testing of the whole system.

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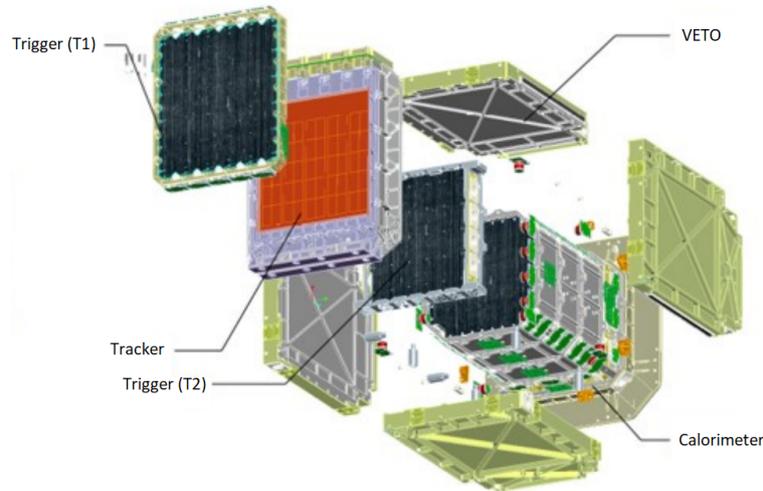*Online – Berlin, Germany*

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*Presenter

Figure 1: HEPD-02 structure

1. The CSES-Limadou mission

The CSES-Limadou mission arises from the collaboration between the China National Space Administration (CNSA) and the Italian Space Agency (ASI) and foresees the realization of a constellation of satellites which will monitor variations in ionospheric parameters that are supposed to be related to earthquakes.

In addition to ASI other italian research institutes and universities take part in the collaboration: the National Institute for Nuclear Physics (INFN), the National Institute for Astrophysics (INAF), the Italian National Institute of Geophysics and Volcanology (INGV) and the Institute of Applied Physics (IFAC).

CSES-Limadou satellites will be equipped with a series of instruments used to detect particles precipitating from Van Allen belts, to measure their energies and to monitor parameters such as the electric and magnetic field and the plasma density.

The first satellite, launched on February 2nd 2018, is currently in orbit and operative while a second one is under development and its launch is scheduled for the late 2023.

The Italian contribution to the second mission consists in the realization of the High Energy Particle Detector (HEPD-02) [1] and the Electric Field Detector (EFD-02).

2. The High-Energy Particle Detector (HEPD-02)

The HEPD-02 will detect electrons and protons in energetic ranges that go from 3 to 100 MeV for electrons and from 30 to 200 MeV for protons.

The structure of the detector, showed in figure 1, can be divided in four sections:

- The trigger system: composed by two segmented planes of plastic scintillator (EJ-200) arranged perpendicularly to each other;

- The tracker section: placed between the two planes of trigger (see figure 1) and composed by a plane of CMOS sensors (ALPIDE), segmented in five parts each of which is composed by three overlapping layers;

- The calorimeter: composed by twelve planes of plastic scintillator followed by two planes of inorganic scintillator (LYSO) arranged perpendicularly to each other;

- The veto system: composed by five planes of plastic scintillator that surround the entire detector.

Each plastic scintillator is coupled with two PMTs (Hamamatsu R9880-210) while LYSO segments with only one PMT, for a total of 64 PMTs.

3. General architecture

The electronics of the detector is composed by four main boards [2][3]:

- The data acquisition board (DAQ), that acquires data from the tracker [4];

- The CPU board, that communicates with the satellite and controls the instrument [5];

- The trigger and PMT readout board (T&PMT), that acquires and digitizes signals from PMTs and produces the trigger signal for the detector [6];

- The telemetry/telecommand board, that controls the power distribution and handles the telemetry and the telecommand signals.

A block diagram of the electronics is shown in figure 2.

The communication between the boards is made by SpaceWire protocol. The satellite communicates with the CPU board using a CAN-bus interface and uses an RS-422 protocol for the DAQ.

The general requirements, common to all the boards, are: low power consumption, passive heat dissipation, radiation hardened components and a redundant design that consists in the realization of two identical copies of the same electronics in order to reduce the risk of critical failures.

4. The trigger and PMT readout board

The T&PMT board is equipped with an FPGA that implements the logic and two ASIC (CITIROC by Weeroc) to acquire the signals produced by the 64 PMTs.

The board is divided in two identical sections (called HOT and COLD). Only one section is normally powered (the HOT section) while the other is used only in case of failures.

Signals from PMTs are not taken from the anode but from the last dynode, in order to have positive signals that are suitable for CITIROCs. An attenuator circuit (the conditioning stage in the diagram) is also needed to match the dynamic input range of the CITIROCs with the amplitude range of PMTs. This is made of resistive voltage dividers designed to guarantee impedance matching with coaxial cables.
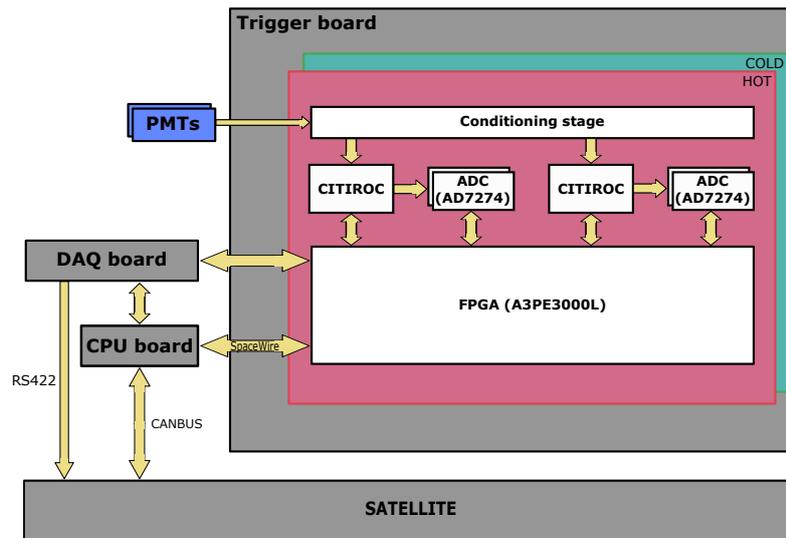
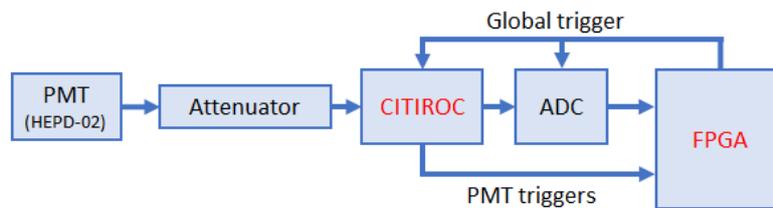**Figure 2:** Block diagram of the trigger and PMT readout board

Figure 3: Operation of the trigger and PMT readout board

The CITIROCs are designed to amplify, shape and store the analog signals and also produce a fast trigger signals for each channel.

The operation of the board is described by the diagram in figure 3 while the schematic of CITIROCs are represented in figure 4.

Both the analog and the trigger signals produced by the CITIROCs are acquired by the FPGA, which applies logic masks and produces a global trigger.

The global trigger enable the readout of the CITIROCs and starts the ADC conversion. The global trigger signal is also sent to the DAQ board to start the acquisition of the tracker. The ADC values are stored in registers and sent to the CPU board.

5. Characterization and measurements

The ongoing work on the board consists in the characterization and optimization of the Engineering Model in sight of the development of the Qualification Model.

A Python script has been written in order to automatize measurements and the analysis of data.

The following activities are in progress:

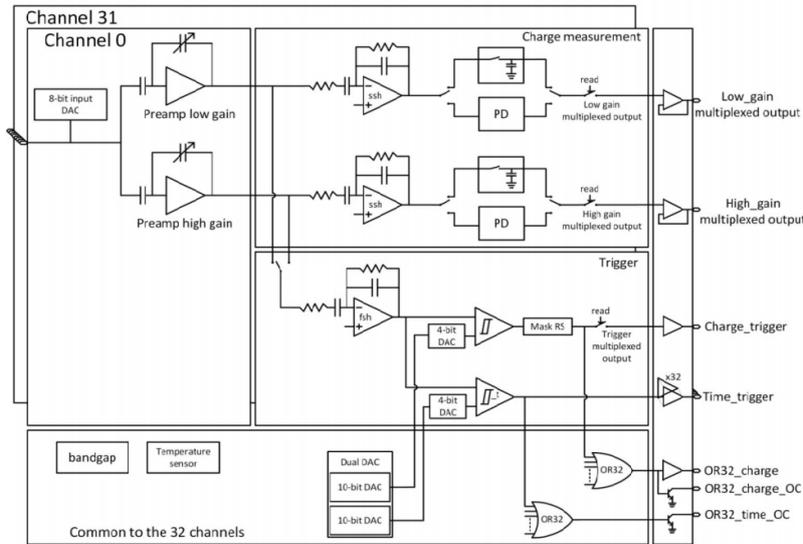- Power consumption measurements and optimization of the power section of the board;

Figure 4: CITIROC schematics [7]

- Threshold and minimum signal amplitude measurements;

- Optimization of every stage of signal conditioning circuit in order to obtain the maximum dynamical range;

- Implementation of improved trigger algorithms with respect to HEPD-01 [8].

5.1 Threshold and minimum signal amplitude

The CITIROC allows to configure a 10-bit DAC to select the threshold for a discriminator (4).

The threshold must be set to a value that allows to reject noise but guarantees the detection of low-amplitude signals (such as those produced by MIPs).

To select a good threshold value a scan of DAC values has been done, using a pulse generator to produce a square pulse with a frequency of 1kHz and increasing the DAC value step by step. The trigger events counted for every DAC value has been plotted and the curve obtained is showed in figure 5a.

The figure shows that a DAC value corresponding to 225 is a good choice to remove the noise. At the selected threshold value another curve has been obtained in order to define the lowest amplitude detectable (the S-curve in figure 5b). The amplitude of pulses has been increased step by step until a 100% trigger efficiency has been reached.

This S-curve shows that signals with an amplitude of 12mV are detected by the board with a trigger efficiency near to 70%.

This value corresponds approximately to 4 photoelectrons produced by a PMT with a gain of $6 \cdot 10^6$.

Given the attenuation value of the conditioning stage (roughly equal to 6), is possible to obtain a threshold of 2/3 p.e. for CITIROCs.
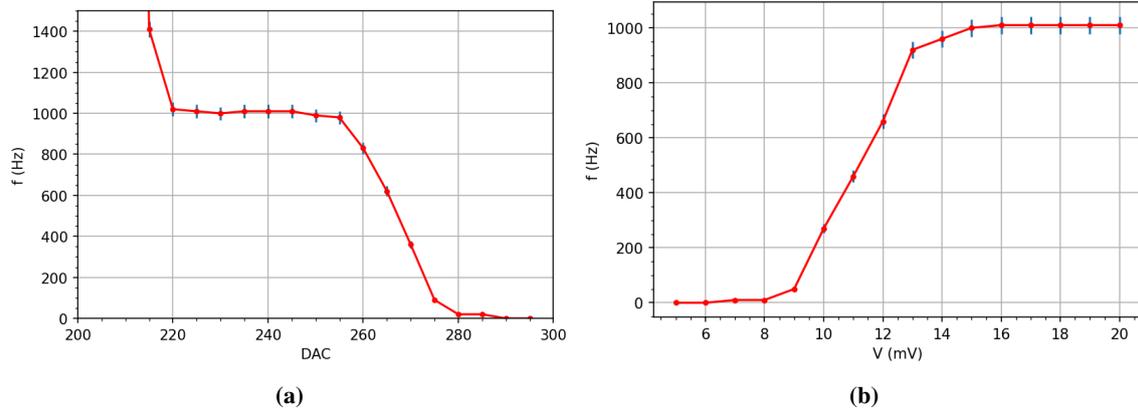
Figure 5: (a) Trigger frequency vs DAC values, (b) S-curve for the minimum amplitude detectable

5.2 PMT readout chain characterization

CITIROC integrated circuits has been chosen for the advantages given by the presence of two independent acquisition lines with different gains. In addition to this is possible to use a Peak Detector circuit instead a Track&Hold system for signal sampling.

The charge measurement section of the CITIROC provide two parallel paths with a preamplifier, a shaper and a peak detector circuit (see figure 4). This two paths (called High Gain and Low Gain) allows to have at the same time two different gain values for input signals.

As previously mentioned, voltage dividers are used for attenuating the PMT signals that need to match the input range of CITIROCs.

Since the maximum signals produced by PMTs have amplitudes around 5÷6V and preamplifiers maximum input are of 1V, an attenuation of 6 has been chosen.

With this attenuation, calibration curves has been obtained for different values of gain and are shown in figures 6a and 6b. These curves show good linearity for input signals up to 800mV for both the High Gain and Low Gain preamplifiers.

In order to obtain the correspondence between the input signals and the ADC values, calibration curves shown in figure 7a and 7b has been obtained for input signals with different widths and for different gains of the Low Gain path. Figure 7a shows the curve for 10ns signals (typical of plastic scintillators) while figure 7b shows 40ns signals curve (the typical width of LYSO crystal signals).

6. Conclusions

The ongoing work on the electronic board used for trigger signal generation and PMT readout, has the purpose of defining operative parameters that will optimize signals acquisition.

A series of measurements and characterization are still in progress in order to have the best possible knowledge of every stage of the PMT readout chain and to use this information for the development of the Qualification Model of the board.
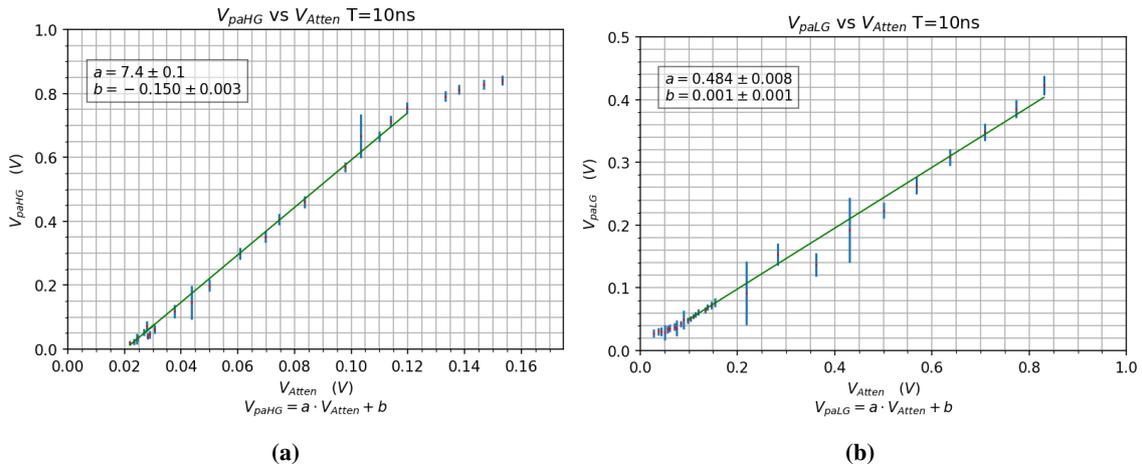
Figure 6: (a) Preamplifier calibration curve for High Gain, (b) Preamplifier calibration curve for Low Gain
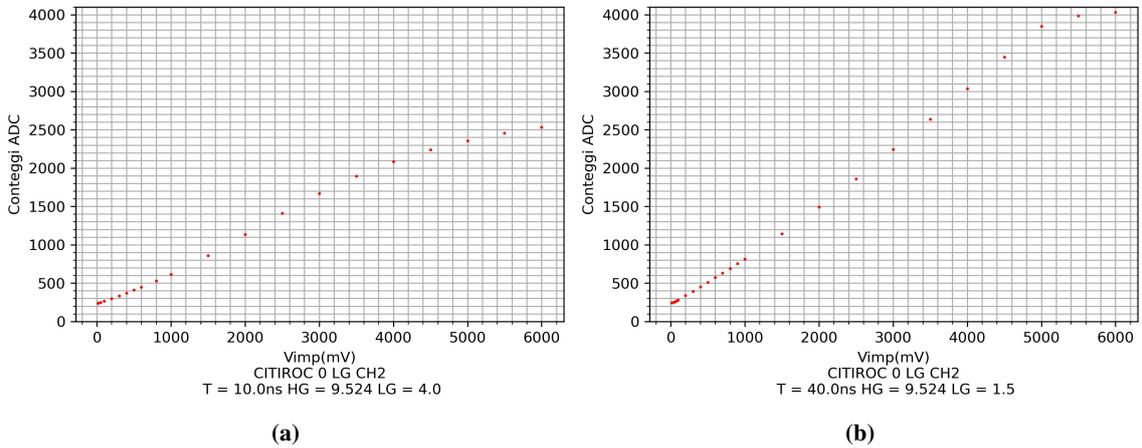

Figure 7: (a) ADC counts vs amplitude for 10ns pulses (b) ADC counts vs amplitude for 40ns pulses

Additional functionalities will be developed to guarantee the correct operation of the detector also in polar regions, in which the particle rate is an order of magnitude higher than that of mid-latitude regions.

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Full Authors List: CSES-Limadou Collaboration

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S. Bartocci[1], R. Battiston[2,3], F. Benotto [4], S. Beolè[4,5], W.J. Burger[3,6], D. Campana[7], G. Castellini[8], P. Cipollone[1], S. Coli[4], L. Conti[1,9], A. Contin[10,11], M. Cristoforetti[12], L. De Cilladi[4,5], C. De Donato[1], C. De Santis[1], F.M. Follega[2,3], G. Gebbia[2,3], R. Iuppa[2,3], M. Lolli[11], N. Marcelli [1,13], M. Martucci[1,13], G. Masciantonio[1], M. Mergè[1,†], M. Mese[7,14], C. Neubuser[3], F. Nozzoli[3], A. Oliva[11], G. Osteria[7], L. Pacini[15], F. Palma[1,†], F. Palmonari[10,11], A. Parmentier [1], F. Perfetto[7], P. Picozza[1,13], M. Piersanti[16], M. Pozzato[11], E. Ricci[2,3], M. Ricci[17], S.B. Ricciarini[8], Z. Sahnoun[11], V. Scotti[7,14], A. Sotgiu[1,13], R. Sparvoli[1,13], V. Vitale[1], S. Zoffoli[18], and P. Zuccon[2,3]

[1] INFN-Sezione di Roma "Tor Vergata", V. della Ricerca Scientifica 1, I-00133 Rome, Italy;
[2] University of Trento, V. Sommarive 14, I-38123 Povo (Trento), Italy;
[3] INFN-TIFPA, V. Sommarive 14, I-38123 Povo (Trento), Italy;
[4] INFN-Sezione di Torino, Via P. Giuria 1, I-10125 Torino, Italy;
[5] University of Torino, Via P. Giuria 1, I-10125 Torino, Italy;
[6] Centro Fermi, V. Panisperna 89a, I-00184 Rome, Italy;
[7] INFN-Sezione di Napoli, V. Cintia, I-80126 Naples, Italy;
[8] IFAC-CNR, V. Madonna del Piano 10, I-50019 Sesto Fiorentino (Florence), Italy;
[9] Uninettuno University, C.so V. Emanuele II 39, I-00186 Rome, Italy;
[10] University of Bologna, V.le C. Berti Pichat 6/2, I-40127 Bologna, Italy;
[11] INFN-Sezione di Bologna, V.le C. Berti Pichat 6/2, I-40127 Bologna, Italy;
[12] Fondazione Bruno Kessler, V. Sommarive 18, I-38123 Povo (Trento), Italy;
[13] University of Rome "Tor Vergata", V. della Ricerca Scientifica 1, I-00133 Rome, Italy;
[14] University of Naples "Federico II", V. Cintia 21, I-80126 Naples, Italy;
[15] INFN-Sezione di Firenze, V. Sansone 1, I-50019 Sesto Fiorentino (Florence), Italy;
[16] INAF-IAPS, V. Fosso del Cavaliere 100, I-00133 Rome, Italy;
[17] INFN-LNF, V. E. Fermi 54, I-00044 Frascati (Rome), Italy;
[18] Italian Space Agency, V. del Politecnico, I-00133 Rome, Italy;
† At ASI Space Science Data Center (SSDC) also, V. del Politecnico, I-00133 Rome, Italy.