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The HEPD-02 Data Processing and Control Unit for the CSES-02 mission

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The China Seismo-Electromagnetic Satellite (CSES) is a multi-instrumental space mission devoted to the study of the ionosphere, with the main aim to investigate possible correlations between fluctuations of the ionosphere environment and the occurrence of an earthquake. The first satellite (CSES-01) was launched on 2018, while a second one (CSES-02) is currently under development and the launch is expected by 2022. As CSES-01, the second satellite includes a particle detector (HEPD-02, High-energy Particle Detector) to measure the increase of the electron and proton fluxes due to short-time perturbations of the radiation belts induced by solar, terrestrial, or anthropic phenomena [1]. The explored energy range is 3-100 MeV for electrons and 30-200 MeV for protons. The HEPD-02 Electronic Subsystem (ELS) contains all the electronics that perform the control of the apparatus and the processing of the signals provided by the sensitive detectors. It consists of the following boards: Trigger, Tracker Data Acquisition (T-DAQ), and Data Processing and Control Unit (DPCU). The DPCU will carry out the functions of management and control of the HEPD-02 operations and the communication with the satellite computer. The DPCU board will implement HOT / COLD redundancy and rely on a Zynq XC7Z7045 Xilinx System on Chip (SoC). The boot and all the functional checks of the SoC will be carried out by a MICROSEMI ProASIC3E FPGA. We present the main DPCU characteristics and functionalities, highlighting the electronic architectural choices to guarantee reliability and radiation tolerance during the entire mission life span.

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1. Introduction

The High Energy Particle Detector (HEPD) is designed to detect electrons in the energy range from 3 to 100 MeV and protons in the range from 30 to 200 MeV with good energy (at least 10% for E > 5 MeV) and angular resolutions (at least 10° for E > 3 MeV) . As already described in [1], HEPD-02 consists of five subsystems:

- **Detector subsystem** (DES): it consists of a tracker based on MAPS sensor plans and a calorimeter based on scintillators read by PMTs;
- **Electronics subsystem** (ELS): carries out all the activities of control, data acquisition and processing, communication with the satellite and housekeeping. The subsystem is composed by three boards: T-DAQ, TRIGGER and DPCU. The TRIGGER and T-DAQ boards are the front-end boards responsible for reading the calorimeter and the tracker respectively.
- **Power supply subsystem** (PSS): it is the subsystem with the task of generating and managing the main power supply voltages of the apparatus. The subsystem is made up of two submodules:LV-PS (in turn made up of two subsystem CTRL-LV and LV-DC/DC) and HV-PS (in turn made up of two subsystem CTRL-HV and HV-DC/DC);
- **Mechanical subsystem** (MES): it is composed of all the structural mechanical elements of the apparatus;
- **Harness subsystem**(HAS): it is composed of all the internal harness and cable.

The DPCU board performs the tasks of managing the communication interfaces towards the satellite (CAN bus and RS-422 communication protocols) and control of all detector operation. In particular, the board implements the following functionalities:

- generation and management of all its internal power supply voltages,
- management of interfaces with the satellite data handling computer (OBDH) for data transfer, telemetry and remote controls (TC / TM),
- reading of scientific and housekeeping data from the other subsystems of HEPD-02,
- packaging and formatting of scientific data,
- management and control of the electronic subsystems of HEPD-02 through slow control links based on spacewire protocol,
- management of safety and recovery procedures in case of system failures/issues.

2. DPCU board Architecture

The DPCU board is based on HOT/COLD redundancy and is divided into three distinct areas: HOT, COLD and COMMON as shown in Figure 1. The HOT and COLD sections are identical and host the same hardware and architecture to implement a cold redundancy scheme (being active one

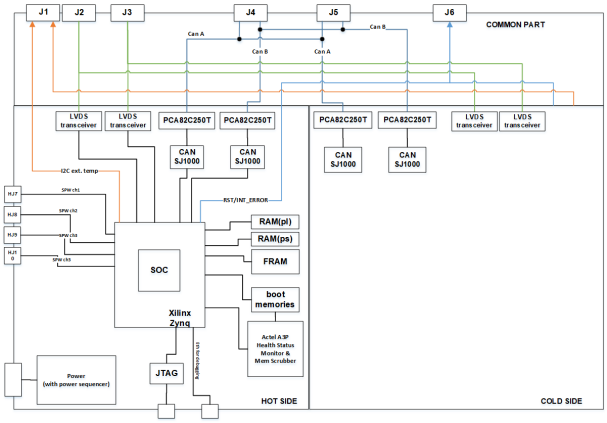


Figure 1: *DPCU board block diagram.*

at a time). The COMMON area hosts all the circuits necessary for the lines impedance matching and the management of the interfaces which are common to both the HOT and COLD sections. As shown in Figure 2, the electronics of the HOT (COLD) areas are based on a Zynq XC7Z7045 Xilinx (XC7Z045-L2FFG900I) System on Chip (SoC) flanked by a MICROSEMI ProASIC3E (A3PE) FPGA. The Xilinx SoC performs the task of control and processing unit while the FPGA has the task of managing the boot of the SoC and performing the role of WatchDog (WD) of the SoC, verifying its correct functioning. To prevent SEU failures in the boot memory, the DPCU board is designed to allow the SoC boot from different boot devices on the board. The DPCU board is designed with the following memory resources usable by the SoC:

- **RAM memory** (DDR): used for processing and data storage operations;
- **Non-volatile memory** (FRAM, Flash): used to store configuration data that must be preserved after a shutdown;
- **BOOT Memories**: non-volatile memories and devices for the boot of the SoC (both firmware and software).

All the on board memories are keep safe with protection and recovery mechanisms (ECC, EDAC etc.). The DPCU board is powered with the 12V voltage received from the PSS subsystem; all the local power voltages necessary for operation are obtained through a conversion section based on a combination of DC/DC converter and low drop voltage regulators in order to maximize the conversion efficiency. The conversion section manage the power-up and power-down sequences and contains the diagnostic circuits and the over-current protection circuits. On each of the HOT/COLD sections of the board, there are two temperature sensors that allow monitoring the board temperature with an accuracy of 0.1° C.

3. DPCU board interfaces

The DPCU board contains the necessary interfaces toward the satellite and for the management of the other 4 control boards of HEPD-02, namely T-DAQ, TRIGGER, CTRL-LV and CTRL-HV. In particular, for each HOT / COLD section, the board contains the following interfaces:

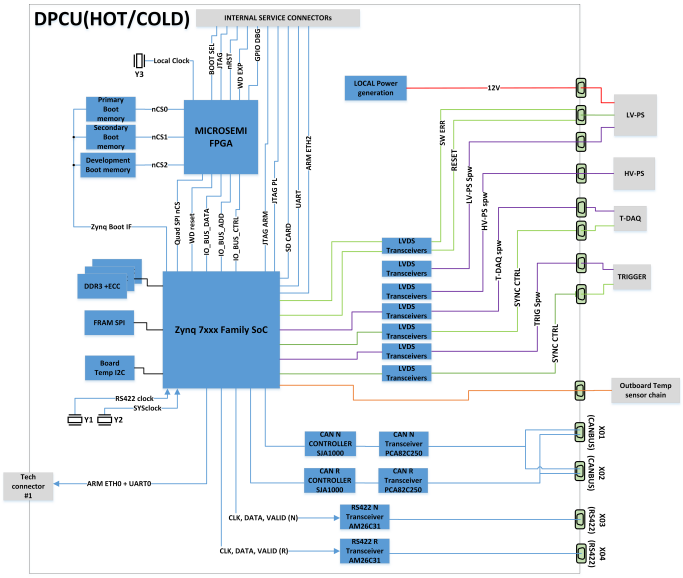


Figure 2: *DPCU electronics architecture block diagram.*

- towards the satellite:
  - two Telecommand/Telemetry CAN-BUS ports;
  - two SCIENTIFIC DATABUS ports (RS-422);
- towards the other electronic board of HEPD-02 ELS and PSS subsystems:
  - four data and slow control spacewire ports;
  - a port with control and synchronization signals to/from TRIGGER board;
  - a port with control signals to/from T-DAQ board;
  - a port with control signals to/from CTRL-LV ;
  - a port for the Detector I2C temperature chain readout;
  - a power supply port from LV-PS (12V input);
- for debugging and service function:
  - one Ethernet link;
  - one UART link;
  - a removable service port with the JTAG interfaces and the SD-CARD slot.

The characteristics of the main and most important interfaces will be described in the following paragraphs.

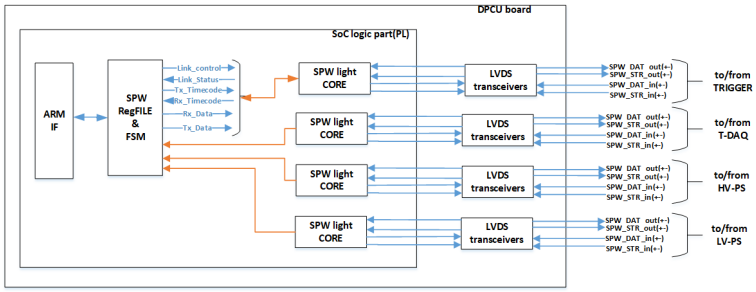


Figure 3: *Block diagram of the Master spacewire IP core node implemented on DPCU.*

3.1 Spacewire interfaces

The spacewire interfaces of HEPD-02 have been developed as an evolution of those present in HEPD-01. In the previous version the spacewire simply performed the task of slow control interface, while in the new device the interface performs the additional task of data transfer interface from the read-out boards (TRIGGER and T-DAQ) by the DPCU. Reusing the architectural choice already experimented and tested in HEPD-01, the management of the four spacewire connections is implemented in the logical part of the SoC while the LVDS physical layers are created through LVDS transceivers mounted on the board. The implemented logic provides four totally independent units in order to ensure parallel and independent access to the subsystems of HEPD-02. The logic of each link involves the use of an open source "spacewire light" core and the logic necessary to allow memory mapped management by the ARM core (Figure 3). In all spacewire control links with peripherals (T-DAQ, TRIGGER, CTRL-LV, CTRL-HV), the DPCU board plays the role of master while all peripherals are slaves. If an error occurs (parity error, disconnection or other error) the state machine attempts to rearm the link. The protocol layer chosen provides a structure formed by command code, address and data.

3.2 CAN bus interfaces(satellite TC/TM bus)

The DPCU board is designed for the management of two CAN bus channels (CAN A and CAN B) with the CAN2.0 standard. As defined in the satellite requirements, in order to ensure redundancy, the board shall be able to manage communication on both channels but it will not have to communicate simultaneously on both CAN buses. The two CAN channels are one nominal and one redundant but always active. Communication from DPCU to satellite on the CAN channel occurs only after a query made by the satellite OBDH computer. The DPCU acts as a slave and has to respond on the same CAN channel used by the satellite. The signals of the CAN A and CAN B channels are present on a single connector which in turn is duplicated to ensure redundancy also on the wiring as indicated in the satellite interface requirements (Figure 4). The CAN bus channels on the DPCU board will use SJA1000 CAN controllers and PCA82C250 transceivers and the nominal bit Rate of the bus will be 307.2 kbps. At the start-up of the DPCU board, the SoC will have to carry out a self-test procedure to check the health status and the correctness of the operations of the CAN bus interfaces.

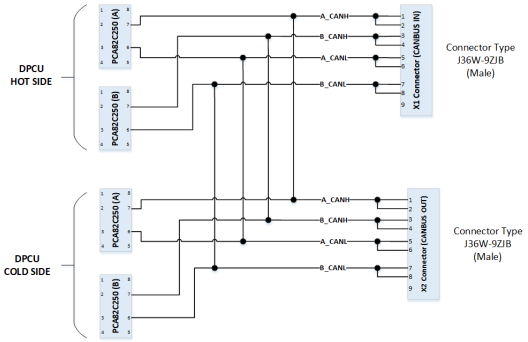
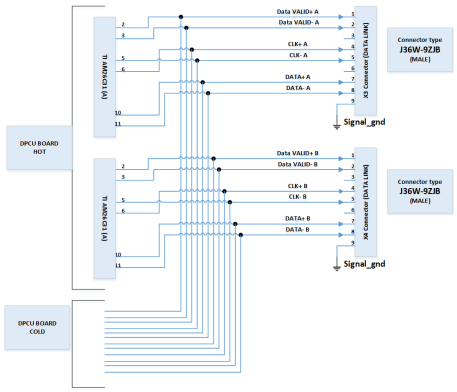


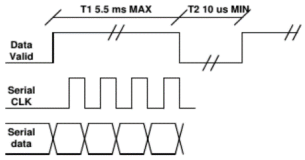
Figure 4: *Block diagram of the interconnections between CAN bus channels on the HOT and COLD side*

3.3 RS-422 interfaces (scientific data bus)

The RS-422 interface of the DPCU card is dedicated to scientific data transfer to the satellite. This interface is developed as a unidirectional (write only) serial peripheral interface (SPI) protocol on a physical layer using an RS-422 transceiver. As defined in the satellite requirements, this interface provides two links, one nominal and one redundant, which simultaneously transmit the data packets (Figure 5a). The physical layer uses the transceiver Texas Instruments AM26C31 already used and validated in the HEPD-01 CPU board. The RS-422 interfaces are characterized by a nominal clock of 6 (± 0.5%) MHz, and the communication timing with a transmission interval T1 of 5.5 ms (MAX) and an inactivity period T2 of minimum 10us, as visible in the timing diagram in Figure 5b.



(a) *Block diagram of the interconnections between RS-422 bus channels on the HOT and COLD side.*



(b) *Timing diagram of the RS-422 scientific data transfer protocol.*

Figure 5: The DPCU RS-422 interface characteristics.

3.4 Control and synchronization interfaces with T-DAQ and TRIGGER boards

For the management and synchronization of event acquisition activities, the DPCU board provides a dedicated interface to the TRIGGER and T-DAQ boards. The following signals are present on the interfaces with the TRIGGER and T-DAQ boards :

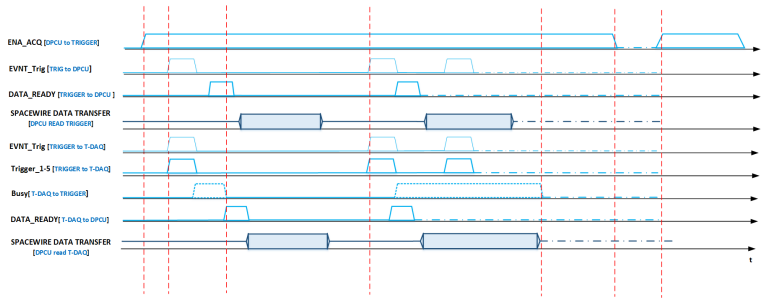


Figure 6: *Timing of Control/Handshake signals between DPCU, TRIGGER and T-DAQ.*

- **Reset** (to TRIGGER and T-DAQ): used by the DPCU to attempt to reset the TRIGGER and T-DAQ boards logic in case of issues.
- **ENA_ACQ** (to TRIGGER): used by the DPCU to block/unblock the events detection activities by the TRIGGER board.
- **EVENT_TRIG** (from TRIGGER): generated by the TRIGGER board to signal the detection of an event.
- **DATA_READY** (from TRIGGER and T-DAQ): generated by the TRIGGER board (and by the T-DAQ board) to signal that an event data packet is ready in the output FIFO.
- **PPS** (to TRIGGER and T-DAQ): generated by the DPCU board to provide a unique time reference for the TRIGGER and T-DAQ boards.

The signals to the two boards are managed by a finite state machines in the logical part of the DPCU SoC; this work jointly with the spacewire finite state machines in order to coordinate both housekeeping and data download activities. The figure 6, shows a time diagram describing the signal activities during the data transfer from the TRIGGER and T-DAQ boards to the DPCU, is shown.

3.5 Control interfaces with CTRL-LV

The interface between the DPCU board and the CTRL-LV board includes the signals involved in the case of start-up problems or anomalous operation of the DPCU software and firmware. These signals come into play both during the power-up phases of the DPCU board and during operation. The signals are generated and managed mainly by the A3P FPGA present on the CTRL-LV and by the A3P PFGA present on the DPCU board.

4. Watchdog management

In order to monitor and manage the correct status of the DPCU, the board is provided with two distinct watchdogs with different timings. A local watchdog is implemented directly on the DPCU board, while an external one is implemented on the CTRL-LV board. The external watch dog carries out a very important activity during the power-up phase of the device. In case the timeout is exceeded, the CTRL-LV board reports the anomaly to the satellite. Once started, the DPCU board

signals its alive status to the CTRL-LV board and then periodically resets the watch-dog counter within the time limit. The reset of the counter is performed through spacewire access, writing a special register on the CTRL-LV. If the watchdog is not reset in time, the CTRL-LV board resets the DPCU board and starts the system reset procedure.

The local watch-dog mechanism implemented on the DPCU board, on the other hand, has the task of detecting any problems on the programmable logics or on the software of the board. In case of any problem, the A3P FPGA signals the anomaly to the CTRL-LV board by asserting a SW_ERROR signal.

5. Electronic components selection

The preselection of the electronic components that can be used for the design of the DPCU board, and in general for all the HEPD-02 electronics sub-systems, required particular attention. Given the high constraints imposed by ITAR on space-qualified components, their re-exportability and usability, and the non-critical radiation profile envisaged for the satellite, the selection of the DPCU board components was mainly carried out on commercial components off the shelf. This choice was also further driven by the positive results of the studies on the usability of commercial components for non-critical space applications, which in recent years, have been increasingly frequent. Furthermore, for the design of the DPCU board, we tried to reuse as much as possible the components already present in HEPD-01, such as: transceivers, FRAM and FLASH memories. With regard to DDR memories, an attempt was made to use components typically employed in previous CERN experiments, where the results of radiation tests (TID and SEU) are well documented. The need to replace the obsolete ADSP2189 processor used in HEPD-01, combined with the results obtained in terms of reliability by SoC-based platforms for CUBESAT, developed by private companies and research institutions (CHREC, gomspace, etc) [2], have guided the choice towards the use of a Xilinx 7000 family SoC as a central control unit. In addition, an attempt was made to use components with automotive qualifications as much as possible in order to take advantage of the intrinsic reliability and the operative temperature range.

6. Conclusion

This paper introduces the architecture of the Data Processing and Control Unit for the HEPD-02 detector that will employed used in the second CSES mission. The design of the board has been completed and its production will start shortly. The enormous flexibility of the architecture and the good computing power make the DPCU board a good tool which could be used in future space missions.

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