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Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

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The Tile Calorimeter (TileCal) is a sampling hadronic calorimeter covering the central region of the ATLAS experiment, with steel as absorber and plastic scintillators as the active medium. The High-Luminosity phase of LHC, HL-LHC, delivering five times the LHC nominal instantaneous luminosity, is expected to begin in 2027. TileCal will require new electronics to meet the requirements of a 1 MHz trigger for Level 1 trigger system, higher ambient radiation, and to ensure better performance under high pileup conditions. Both the on- and off-detector TileCal electronics will be replaced during the shutdown of 2024–2027. PMT signal from every TileCal cell will be digitized and sent directly to the back-end electronics, where the signal is reconstructed, stored, and sent to the Level 0 trigger at a rate of 40 MHz. This will provide better precision of the calorimeter signals used by the trigger system, compared to the current system, where analog trigger sums are used. In addition, it will allow the development of more complex trigger algorithms. The modular front-end electronics feature radiation-tolerant commercial off-the-shelf components and redundant design to minimise single points of failure. The timing, control and communication interface with the off-detector electronics is implemented with modern Field Programmable Gate Arrays (FPGAs) and high speed fiber optic links running up to 9.6 Gbps. The TileCal upgrade program has included extensive R&D and test beam studies. A hybrid Demonstrator module which has both new readout architecture and reverse compatibility with the existing system was inserted in ATLAS in August 2019 for testing in actual detector conditions. The ongoing developments for on- and off-detector systems, together with expected performance characteristics and recent results of test-beam campaigns with the electronics prototypes are presented here.

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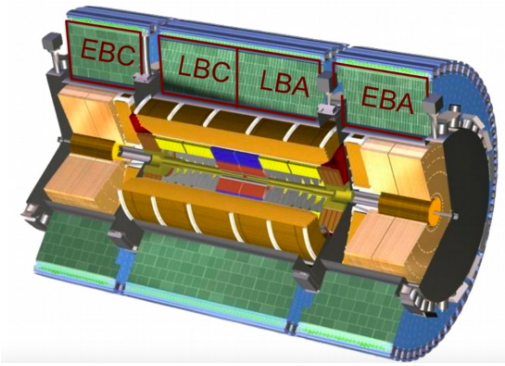
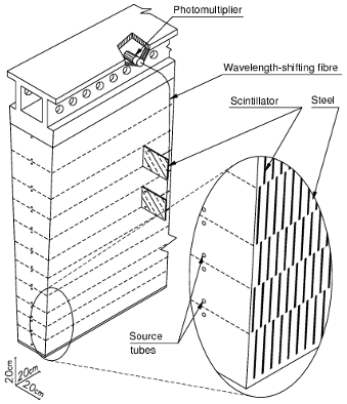
1. Introduction

The Tile Calorimeter (TileCal) [1] is the hadronic calorimeter of the central region of the ATLAS experiment [2] at the Large Hadron Collider (LHC) at CERN. The TileCal was designed to achieve high performance in energy reconstruction of hadrons, jets, tau-particles, and missing transverse momentum. TileCal is a sampling calorimeter which uses steel plates as passive absorber along with plastic scintillators as the active medium. As shown in Figure 1a, TileCal is composed of three cylinders: one long central barrel which is divided into LBA and LBC, in addition to two extended barrels (EBA and EBC). Each of the four sections are subdivided azimuthally into 64 wedge modules (see Figure 1b), creating a total of 256 modules. Charged particles produce light in plastic scintillators, which is then fed to photomultiplier tubes (PMTs) by the wavelength shifting fibers. The readout of the calorimeter is grouped into pseudo-projective geometry cells. Each cell is being read by two PMTs. Each module in the long barrel has up to 45 PMTs, while the modules in the extended barrels only have 32 PMTs.



(a) The entire TileCal within ATLAS, composed of three cylinders of long barrel, and two extended barrels.



(b) One wedge section (module) of the TileCal.

Figure 1: Structure of the Tile Calorimeter [3].

During the high luminosity phase of LHC (HL-LHC), the instantaneous luminosity will increase up to 7.5×10^{34} cm^{-2}s^{-1}, which is five times higher than the nominal LHC luminosity [3]. This produces up to 200 collisions per 25 ns bunch crossing, and causes an increase in the ionizing dose received by the on-detector electronics up to 80 Gy for 4 ab^{-1}. The increased radiation levels, higher trigger rates and pileup conditions, along with ageing of some of the components are the main reasons for the upgrade of the TileCal and its elements.

2. Overview of Tile Calorimeter Upgrade for HL-LHC

In general, a fully digital trigger system with higher granularity and precision, compared to the current system will be used. All data will be sent to the Level 0 (L0) trigger system at 40 MHz. The system requires 2048 optical links running at 9.6 Gbps from on-detector electronics to the back-end electronics in the counting rooms. The effective dynamic range of digitization will be increased from 16 bits to 17 bits. On-detector electronics will be more radiation tolerant. For example,

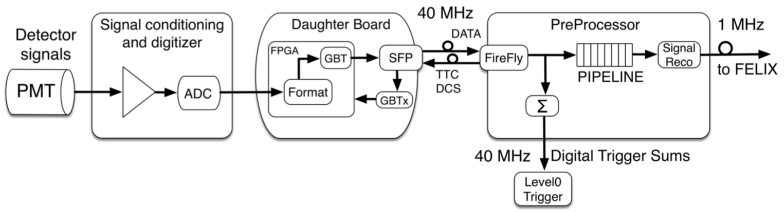


Figure 2: Upgraded readout chain of the TileCal [4].

the on-detector FPGAs are sensitive to Single Event Upsets (SEUs). Therefore, a triple redundant scheme is adopted. In general, many redundancy levels have been considered. Mini-drawers are logically split into two sides, and each cell is read out by two independent PMTs. In case of a failure, the dead region would be one-eighth compared to the current system. Due to ageing and significant degradation of some PMTs, around 10% of them, covering the most exposed cells, will be replaced. Low voltage will be regulated locally on front-end electronics using point-of-load (POL) regulators. In addition, high voltage will be regulated remotely in the counting room, USA15.

3. Upgrade of Tile Calorimeter Components

In the current system, the PMT signals are shaped, amplified, and digitized at 40 MHz using a clock that is synchronized with the beam crossing. These digital samples are stored in pipeline memories on the front-end electronics for the duration of Level 1 (L1) trigger latency (2.5 μs). In addition, the PMT analog signals are grouped and transmitted to the Level 1 Calorimeter system. Then, the digital samples selected by the L1 trigger system are transmitted to the Read-Out Drivers (RODs) in the back-end electronics at an average rate of 1 kHz. However, in the proposed upgraded system, the readout chain has been changed to cope with the HL-LHC conditions, such as higher trigger rates and pileup (see Figure 2) [4]. As seen in this figure, after being shaped, amplified, and digitized at the same clock of 40 MHz, the PMT signals will go through FPGAs to be sent to back-end electronics using optical fiber links running at up to 9.6 Gbps. The digital trigger sums will then be created in the back-end electronics and sent to the L0 trigger system. This fully digital readout will provide more granular and precise trigger system with respect to the current design, and will allow for the development of more complex trigger algorithms. The pipeline memories, which are moved to the back-end electronics, are capable of coping with latencies and rates of the new trigger system. Upon acceptance from the L0 trigger system, the selected samples will be sent to Front End LInk eXchange (FELIX) within the global ATLAS DAQ system at a rate of 1 MHz.

PMT Block and HV Divider: PMTs are located inside the PMT blocks, converting the light to electric signals. 768 PMTs will be replaced due to ageing. The HV dividers are sitting on the end of PMTs, dividing the input HV and providing voltages for PMT dynodes. The DC anode current can go from a maximum of 8 μA in LHC to 40 μA in HL-LHC. Therefore, linearity in response of the PMTs is important. Active dividers, which contain transistors and diodes in addition to passive components, are replacing passive dividers to provide better response linearity for HL-LHC.

FENICS: Located on top of active dividers are FENICS boards, which shape PMT pulses and prepare them for the ADCs on the mainboard by two gains. They also provide slow integrator signal

for energy calibration and luminosity monitoring. The gain ratio of the outputs of FENICS is 40 (the signal is attenuated/amplified by gains of 0.4 and 16). Selected gains provide a saturation limit of 1050 pC (1 TeV) for the low gain signal.

Mainboard and Daughterboard: Located inside the modules of the detector, the mainboard hosts a daughterboard. The mainboard receives data from FENICS, digitizes it, and passes it to the daughterboard. The new version of the mainboard features voltage and current monitoring to be sent to counting rooms. The daughterboard formats the data and sends it to the back-end electronics through optical links. Major changes in the daughterboard include using Kintex Ultrascale FPGA with improved power sequencing, improved routing from mainboard ADC to achieve better readout timing performance, and added protection circuits against over-current.

PreProcessor: Located in the counting rooms, the PreProcessor (PPr) receives data from the detector and computes energy and time for each channel. Unlike the current system with on-detector data pipelines, the pipeline buffers are moved to PPr. As the buffers are closer to the trigger system, there will be lower propagation delays. PPr is composed of CPMs (Compact Processing Modules) hosted by an ATCA (Advanced Telecommunications Computing Architecture) carrier board. A custom ATCA carrier is also designed to host the CPM and provide a connection between the CPMs and Trigger and Data AcQuisition interface board (TDAQi).

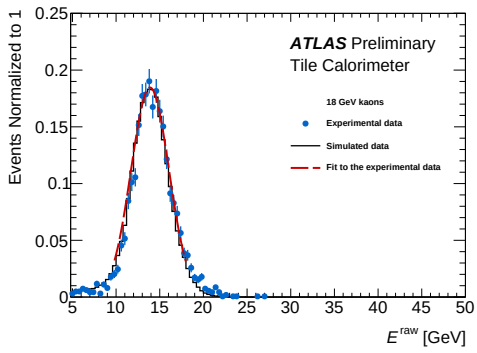
TDAQi: Sitting inside an ATCA crate, the TDAQi receives channel energies from the PPr and computes cell energies and quantities to be passed to the L0 trigger. Digital trigger sums in TDAQi are replacing analog trigger sums, which was being done on-detector.

Mechanics: All of the front-end electronics are placed on mechanical structures called super-drawers, to be inserted inside three-meter-long girders. For the upgraded system, mini-drawers have been designed with half of the length of the current drawers, which provides better accessibility and robustness, and reduces the number of possible single points of failure. The design of the super-drawers is different for long barrels and extended barrels, since the extended barrel modules have fewer PMTs than the modules of the long barrel. This tailored design for extended barrel modules, will decrease the number of front-end electronic boards.

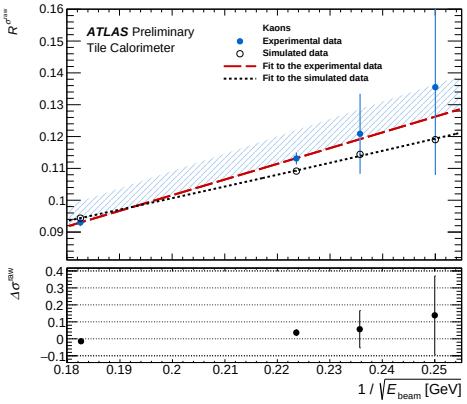
High Voltage Distribution System: The HV distribution system provides regulated high voltage for individual PMTs considering requirements like noise, ripple, and temperature dependence. Unlike the current system, where the regulation is being done on detector, in the upgraded HV system, the regulation is being done remotely in the counting rooms. This eliminates the radiation hardness requirements and provides much better accessibility. Each of the HV regulation boards provides 48 outputs for individual PMTs in each module.

Low Voltage Distribution, Control, and Monitoring System: Unlike the current 2-stage LV distribution system, where different voltage levels are being provided to the front-end electronics by the LV box, the upgraded LV distribution system is composed of 3 stages. All LVPS bricks provide 10 V to the front-end electronics, which will be converted by POL regulators to different voltages needed by the electronics. There were several radiation test campaigns on LVPS bricks. As a results of these tests, some of the brick components were replaced with more radiation tolerant counterparts. In addition, new test stations have been developed to fully test the bricks after production [5].

Monitoring of the bricks is being done by ELMB (Embedded Local Monitoring Board), hosted by an ELMB motherboard inside the LV box. The ELMB motherboard has been redesigned to



(a) Distributions of the reconstructed energy E^{raw} obtained analyzing kaon data.



(b) Energy resolution normalized to incident beam energy.

Figure 3: Study on test beam results for kaons with 18 GeV hadrons [6].

be compatible with the new tri-state control method of the LVPS bricks, and is very robust and radiation tolerant. The off-detector Auxiliary boards were also recently redesigned to provide the new tri-state control signals to the bricks.

Calibration Systems: The two main calibration systems of TileCal are Cesium (Cs) and laser, which are used to calibrate the scintillators and PMTs, respectively. The Cs system is composed of a ^{137}Cs source, driven by a liquid through all tiles, to deposit well controlled energy flux in the cells. New control boards of the Cs system are designed with higher radiation tolerance and new optical link interface with the Detector Control System (DCS). The Laser system uses 400 clear fibres (100 m long) splat and routed to all PMTs, to feed the laser light to the modules. In addition to new board for control and interface with TDAQ and DCS, the light mixer in the current system will be replaced by an integrating sphere to add controlled source of DC light to simulate underlying minimum bias events during the calibration.

4. Test Beam Results

Several test beam campaigns have taken place since 2015 to test and validate the proposed electronics for the upgrade of TileCal, during which interesting performance results have been obtained. As an example, a study that was done on TileCal response to kaons [6] is presented here. A beam of mixed hadrons at the energy of 18 GeV was used. Energy distribution of 18 GeV kaons is shown in Figure 3a. The shower energy E^{raw} is the sum of energy deposited in all calorimeter cells. The blue dot histogram represents the experimental data, while the dashed curve in red corresponds to the fit of a Gaussian function to the experimental data in a region $\pm 2\sigma$ around the peak value. The black histogram corresponds to the simulated data. The mean energy is less than the beam energy of 18 GeV, which is due to the non-compensating nature of the calorimeter. In Figure 3b, the normalized energy resolution, $R^{\sigma^{\text{raw}}}$, is shown as a function of $1/\sqrt{E_{\text{beam}}}$ for both experimental data (blue dots) and simulated data (black circles). The red dashed (black dot) curve corresponds to a fit to the experimental (simulated) data points. In addition, a quantitative comparison between experimental and simulation results is presented.

5. Demonstration Insertion

During several test beam campaigns, a hybrid demonstrator module was prepared and tested, which offers both backward compatibility with the current modules (analog trigger signals) and upgraded readout system with digital trigger signals. This module was finally inserted in the detector in July 2019 during the LS2 (Long Shutdown 2), and replaced a legacy module in the long barrel (LBA14). This module is composed of four mini-drawers with 45 PMTs and legacy 3-in-1 cards (instead of FENICS), HV dividers, mainboards, daughterboards, adder base boards, and trigger adder cards, in addition to the upgraded LV box and HV distribution board. Moreover, in the counting room, a PPr demonstrator inserted in an ATCA carrier, upgraded LV control system and HV remote boards were installed. The demonstrator module is now fully integrated in TDAQ, and shows lower noise compared to the legacy modules, thanks to its larger dynamic range.

6. Summary

Extensive R&D work has been performed in order to upgrade the ATLAS TileCal for the high luminosity LHC. The readout resolution, sensitivity, and dynamic range will be slightly improved. Special attention is given to redundancy, reliability, and radiation hardness of the components. The fully digital readout scheme will allow for using greatly enhanced trigger capabilities. Improved monitoring and calibration capabilities are also enforced. Extensive tests of the design have been performed with the SPS beams since 2015. The demonstrator module, which is backward compatible with legacy modules, was inserted in the detector in 2019, and will be included in LHC Run 3.

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