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ATLAS Level-0 Endcap Muon Trigger for HL-LHC

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The status of the development of the Level-0 endcap muon trigger system for the ATLAS experiment at the HL-LHC is presented. The upgraded system reconstructs muon candidates with an improved p_{T} resolution by combining data from various subdetectors. This is realized by exploiting the evolution of the data transmission technologies, to send all hit data of Thin Gap Chambers (TGCs) and the data of other subdetectors to the counting room. Primitive muon candidates are reconstructed using track segments reconstructed from hit data of TGCs. An initial implementation of the TGC track segment reconstruction with firmware for an FPGA is tested, and it is verified that muon candidates are successfully reconstructed for ideal cases. The trigger efficiency is estimated with a software algorithm and using a Monte Carlo simulation. The efficiency is estimated to be higher than 90% for the threshold of $p_{\mathrm{T}} > 20$ GeV and the endcap region. The trigger rate is estimated with a software algorithm and using pp collision data, which are overlaid to emulate the high pileup condition at the HL-LHC. The rate is estimated to be lower than 25 kHz for the threshold of $p_{\mathrm{T}} > 20$ GeV and the endcap region. This evaluation does not include the precise determination of p_{T} using Monitored Drift Tube (MDT) hits, and the trigger rate is expected to decrease with its inclusion.

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1. Introduction

To cope with the higher pp collision rate of the High-Luminosity LHC (HL-LHC), the trigger and readout systems of the ATLAS detector [1] will be replaced [2], including those for the muon system. The bunch crossing rate is 40 MHz, and the baseline of the hardware trigger is a maximum rate of 1 MHz and 10 μs latency. Recent R&D results of the Level-0 endcap muon trigger are reported.

2. Level-0 endcap muon trigger

ATLAS muon system is composed of several gaseous subdetectors. The layout for the HL-LHC phase is shown in Figure 1. The Thin Gap Chamber (TGC) is a multiwire proportional chamber that has small distances between the anode wires and readout cathode strips for fast time response. The Monitored Drift Tube (MDT) is a gaseous drift chamber for precise measurements of muon tracks. The Resistive Plate Chamber (RPC) provides hits with fast time response. The New Small Wheel (NSW) is a new subdetector planned to start its installation in 2020. The NSW uses two chamber technologies: TGCs with small strips and Micromegas detectors. Additionally, the Tile hadronic calorimeter is utilized for the endcap muon trigger, as described later. It is a sampling calorimeter with steel absorbers and plastic-scintillator tiles.

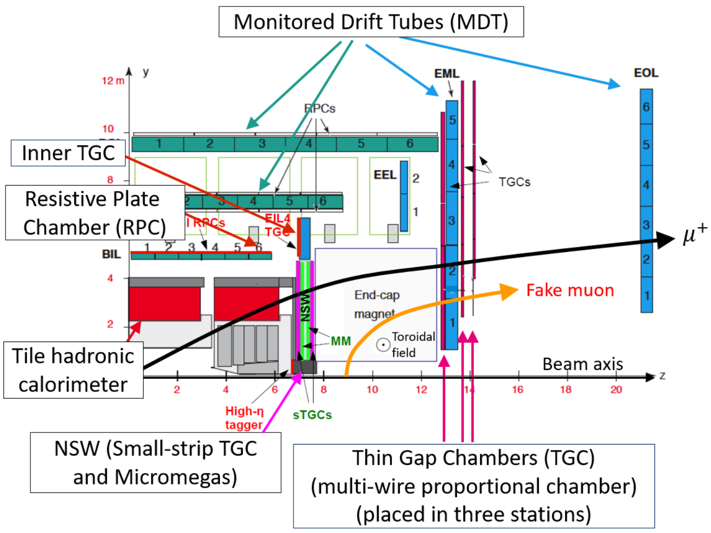

Figure 1: The layout of the ATLAS subdetectors for the HL-LHC phase, shown in the $R-Z$ plane [3]. It is shown for one of the azimuthal sectors that are in-between the barrel toroid coils ("large sector").

The ATLAS endcap muon trigger for the current system, i.e. that used for Run 2 from 2015 to 2018, uses simple coincidence logic in the TGC frontend boards and performs p_{T} evaluation in the backend boards using look-up tables.

From Run 4, which begins from 2026, a new hardware-based (Level-0) endcap muon trigger will be installed to reduce the trigger rate and to keep high trigger efficiency. The key feature of this upgrade is the reconstruction of muon candidates with an improved p_{T} resolution. This is realized by exploiting the evolution of data transmission technologies; all hit data of TGCs are sent to the counting room after bunch identification. Also, data of inner subdetectors (inner TGC, NSW, RPC, Tile hadronic calorimeter) are sent to the counting room. Although the Tile hadronic calorimeter is not a component of the muon system, it is utilized here to improve the coverage in the ϕ direction. The muon candidates are reconstructed in the backend boards placed in the counting room. Primitive candidates are reconstructed based on hits in the TGC detectors. The p_{T} of the muon candidates is determined from the difference of positions and polar angles between track segments in TGC and data in inner subdetectors. Further, the precise determination of p_{T} is performed using track segments in MDT.

"Fake muons" are low-p_{T} charged particles coming from the beam pipe that may be reconstructed as muon candidates, as shown in Figure 1. The contribution of fake muons is removed by taking a coincidence of track segments in TGC and data from inner subdetectors.

3. Hardware implementation

The logic of the Level-0 endcap muon trigger is implemented in a backend board ("Endcap Sector Logic board") housed in an ATCA shelf. It performs several tasks, including the reconstruction of muon track segments in TGC, taking coincidence with other inner subdetectors, and the data readout. For the FPGA of the board, the Xilinx Virtex UltraScale+ FPGA (XCVU9P) is considered. This FPGA has approximately a hundred pairs of GTY transceivers, which are suited for receiving data from various subdetectors. It also has a huge memory resource (UltraRAM) that is suited for the track reconstruction. Forty-eight boards are used for the whole system.

The reconstruction of muon track segments in TGC is an important process to determine primitive muon candidates. The TGCs in the region 13 m $< |z| <$ 16 m (the "Big Wheel" region) are placed in three stations, as shown in Figure 1. The hits in these TGCs are used for the track segment reconstruction. The reconstruction is based on a pattern-matching method, where the θ and p_{T} of the muon track segment are determined using a predefined pattern list stored in the RAM of the FPGA.

Initial test of the firmware implementation of the muon track segment reconstruction using TGC hits is performed. The Xilinx Virtex UltraScale+ evaluation board (VCU118) is used. TGC hits from Monte Carlo simulation of single muons are used as input test vectors. The p_{T} and η of the simulated muons are $p_{\mathrm{T}} = 20$ GeV and $2.13 < \eta < 2.16$. Only ideal events with exactly one hit on each of the seven TGC layers (i.e. seven hits in total) are selected, and 1000 events are tested. As a result, the track segment is reconstructed successfully for all 1000 events. The relationship between the polar angle of the obtained track segment and that of the segment obtained from an offline reconstruction using MDT hits is shown in Figure 2. The result is consistent with that obtained from a software simulation.

The estimated usage of the RAM resource for the entire channel list is approximately 100 Mbit, which is one-third of the RAM resource of XCVU9P FPGA.

4. Performance evaluation with software algorithm

The performance of the Level-0 endcap muon trigger is evaluated. The evaluation excludes

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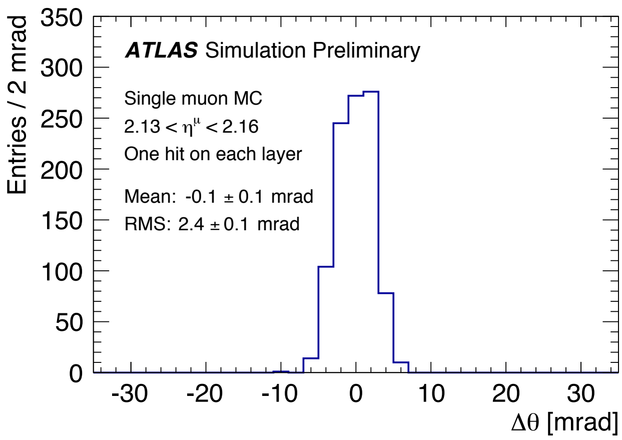


Figure 2: The distribution of the polar angle difference $\Delta\theta$ [4]. $\Delta\theta$ is the difference between the polar angle of the track segment obtained from the TGC hits using a pattern matching method implemented in the firmware of the FPGA and that of the track segment obtained from an offline reconstruction algorithm based on MDT hits.

the precise determination of p_T using MDT hits.

The trigger efficiency is evaluated using Monte Carlo simulation of single muons at the HL-LHC condition. It is evaluated for muons in the region $1.05 < |\eta| < 2.4$. The result is shown in Figure 3. The estimated efficiency is higher than 90%, which is higher than the current Run 2 system; this is because of the looser coincidence condition used compared to the Run 2 system. Also, the rejection of low-p_T muons is better (i.e. the trigger efficiency for muons with $p_T <$ 20 GeV is lower) compared to the Run 2 system because of the improved p_T resolution.

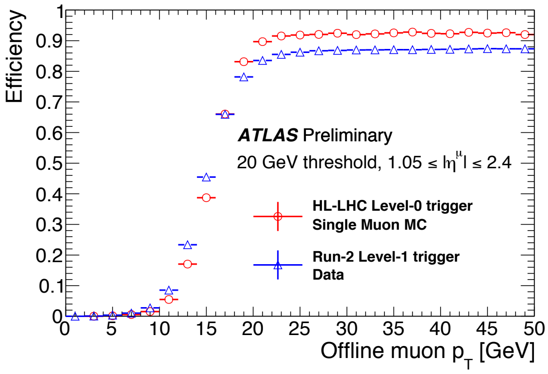
The trigger rate for the high pileup (up to 200) condition of the HL-LHC is evaluated using collision data recorded with a zero-bias trigger in 2016 during Run 2. The high pileup condition is emulated by overlaying collision data. The result is shown in Figure 3. For $p_T > 20$ GeV, which is the primary threshold for the single-muon trigger, the trigger rate for the endcap region is lower than 25 kHz.

5. Demonstration of data transfer using clock data recovery

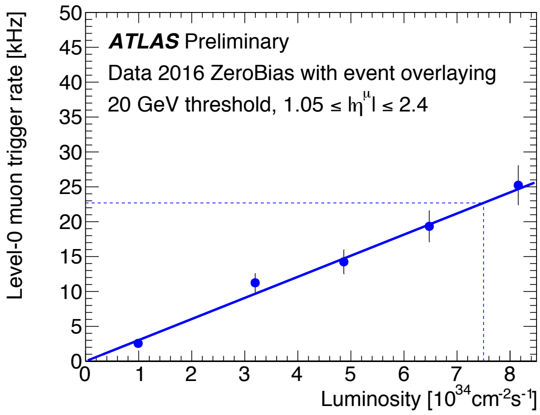
The frontend board of the TGC sends the TGC hit data to the Endcap Sector Logic board via optical cables using 8b/10b encoding. The 40 MHz clock synchronized to the accelerator clock is provided from the Endcap Sector Logic board to the frontend boards via optical cables, and the clock data recovery unit inside the FPGA is used to generate the 40 MHz clock. The data transfer using the clock data recovery is tested, using a prototype of the TGC backend board and an Endcap Sector Logic board developed for Run 3. No bit error was detected, and the corresponding upper limit on the Bit Error Ratio is 5×10^{-16}.

6. Summary

Recent R&D results of the ATLAS Level-0 endcap muon trigger for the HL-LHC are pre-



(a)



(b)

Figure 3: The estimated performance of single-muon trigger with a threshold of $p_{\mathrm{T}} > 20$ GeV for the HL-LHC condition [4]. (a) The trigger efficiency is estimated using a Monte Carlo simulation. It is estimated for muons in the range $1.05 < |\eta| < 2.4$, and it is presented with respect to the value of p_{T} obtained from the offline reconstruction algorithm. Additionally, the trigger efficiency for the Run 2 condition, that is obtained from the collision data recorded in 2018, is shown for comparison. (b) The trigger rate is estimated using collision data collected in 2016 with a zero-bias trigger. The trigger rate is evaluated for muons in the range $1.05 < |\eta| < 2.4$. The track segments obtained from MDTs are used to emulate the track segments obtained from the NSW.

sented. The system combines all hit data of TGCs and the data of inner subdetectors (inner TGC, NSW, RPC, Tile hadronic calorimeter), with the aim to reconstruct the p_{T} of muon candidates with high precision. An initial test of the firmware implementation for the track segment reconstruction based on TGC hits is performed. It is verified that muon candidates are successfully reconstructed for ideal cases. The trigger performance is estimated using a software algorithm, and it is evaluated to have an efficiency higher than 90%, and a rate lower than 25 kHz, for muons entering the region $1.05 < |\eta| < 2.4$. For this evaluation, the precise determination of p_{T} using MDT hits is not included, and the trigger performance is expected to improve with its inclusion.

References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *JINST* **3** (2008) S08003.

[2] ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2017-020. ATLAS-TDR-029, CERN, Geneva, Sep, 2017.

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[4] ATLAS Collaboration, "Level-0 TGC Trigger Performance of trigger algorithms in software and firmware implementations."
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