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Study of SEU effects in circuits developed in 110 nm CMOS technology

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Channel configuration registers of a full size prototype for the custom readout circuit of silicon double-sided microstrips of PANDA Micro Vertex Detector were tested for upset effects. The ASIC is developed in a commercial 110 nm CMOS technology and implements both Triple Modular Redundancy and Hamming Encoding techniques. Results from tests with ion and proton beams show the robustness level of these two techniques against the upset effects and allow the evaluation of that commercial 110 nm technology in the PANDA experiment.

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1. Introduction

The INFN-Torino has developed ASICs for readout applications of detectors in many different technologies. Among them a commercial 110 nm CMOS technology. This technology has the advantage of a relatively low cost which makes it suitable even for small projects. The drawback is that it is lacking a systematic characterization of its radiation tolerance. First tests of Total Ionizing Dose have already been done [1].

The first ASIC designed at INFN-Torino in this technology was the prototype named PAStA [2] (PANDA Strip ASIC) for the readout of silicon micro-strips configuration for the Micro Vertex Detector (MVD) of the PANDA experiment [3]. It was developed by a JLU Gieβen, FZ Jülich and INFN Torino collaboration. Since it implements the two typical methods [4] to mitigate the Single Event Upset (SEU) effects, Triple Modular Redundancy (TMR) technique and Hamming Encoding, it is a good candidate to investigate the behaviour of that commercial 110 nm technology in a radiation environment. These techniques have been already studied in previous projects, developed at INFN-Torino, based on a 130 nm CMOS technology from a different manufacturer and a slightly higher tolerance to the radiation of TMR with D type flip flop circuits was observed [5] [6] [7].

In general, TMR may be preferred when die size and power values are not a problem in the project, two requests that are often rather stringent in the electronics associated with silicon sensors for a vertex detector as it is in the case of PAStA circuit. Two assessments were conducted using PAStA as device under test, the first one using ion beams to evaluate the cross section for upset effects and the second one using proton beams to perform a direct measurements of upset rate.

2. PAStA and the experimental setup

PAStA (Figure 1) is a full size chip fabricated on a Multi Project Wafer in 110 nm CMOS technology.

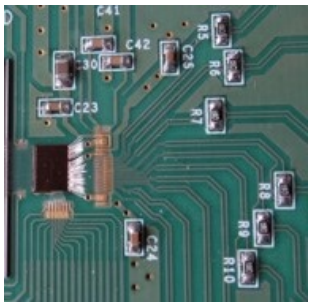

Figure 1: PAStA circuit (on the left of the picture) wire bonded to its test board

The circuit features a nominal clock frequency of 160 MHz. It implements 64 readout channels and uses the Time over Threshold (ToT) technique to determine the charge information by a measurement with an 8 bit resolution. Its concept is derived from TOFPET, developed to read out Silicon Photo Multipliers in a Time-of-Flight PET application [8]. Each channel contains three distinct building blocks: an analog front-end, an analog TDC and a digital TDC controller. A global controller merges the data from all the channels and distributes the configuration information. Ten

LVDS links communicate to the outside. The chip hosts the bias cells of the analog stages and a calibration circuit, generating a test pulse with configurable amplitude. The analog front-end implements a specific design to cope with micro-strips sensors, radiation hardness protection techniques have been implemented as well [4].

The analog front-end consists of four stages [9]: the charge sensitive amplifier, the current buffer, the ToT amplifier and the comparator.

The charge sensitive amplifier has two feedback networks implemented to process signals coming from both p- and n-type silicon strips. The current buffer provides a current amplification and an impedance adaptation, while the ToT amplifier discharges a feedback capacitance with a constant current. The comparator is a dual threshold hysteresis circuit, its lower threshold secures the leading edge of the signal to get the event timestamp, while the higher threshold works on the signal falling edge for the ToT measurement purpose. Its output signal is used by a local controller to drive the TDC with an analog interpolator circuit equipped with a Time to Amplitude converter and a latched comparator. As for the analog TDC, the digital blocks of PAStA are adapted from TOFPET [8], with the major changes being the introduction of radiation protection techniques and a general optimization for the specific application.

Several registers are implemented in each channel: 13 single bit registers, additional 29 bits distributed on 8 registers featuring different length of bit words (2, 4 and 5 bits). To protect these circuits from SEU effects, two different techniques were implemented: TMR on single bit registers and Hamming encoding on multiple bits registers.

The chip prototype is mounted on a dedicated test board (provided by the group from JLU Gieβen, involved in the PANDA MVD project) that hosts all the necessary power regulators, the reference voltages and the interface to all the LVDS and single-ended signals. The board also offers the possibility to mount a strip sensor and to connect it with wire bonding to the PAStA input channels. It was used to characterize the circuit using a radioactive source [2] and a proton beam [10] at FZ Jülich.

A dedicated DAQ in LABView has been developed to configure the ASIC registers and acquire data. It is a standalone setup based on a Xilinx Virtex 6 ML605 Evaluation Board. Each channel requires to be configured with a sequence 42 bit long. For the SEU evaluation a balanced sequence made of 1 and 0 is sent to the chip to set up each channel. The tests are performed following this procedure: a writing command is followed by a reading phase until a SEU is detected showing an inefficiency of the TMR circuit or Hamming Encoding technique, then the cycle starts again from the beginning. The acquisition program counts the number of times when the bit changes its value (1-0, 0-1), therefore it records the number of errors which have been detected.

3. Tests and results

To evaluate the cross section for upset effects of the channel configuration registers, PAStA was irradiated with ion beams at the SIRAD facility at INFN-LNL. The PAStA testing board is placed inside a vacuum chamber (Figure 2) and about two meter long cables connect this board to the Xilinx Virtex 6 ML605 board placed outside the chamber and connected to the computer. This setup limits the clock frequency to 50 MHz.

Figure 2: PAStA test board installed in the Vacuum Chamber of the SIRAD facility

The SEU cross section is evaluated as the ratio between the number of detected upsets with respect to the ion fluence per cm^2 (the fluence is known with a 10% error) and normalized by the bit number of the 64 configuration words (2688 bit). Data for seven different type of ions are plotted in Figure 3 as a function of their Linear Energy Transfer (LET) values. However the SEU cross section value for a proton environment, derived from the convolution with the probability of energy deposition from protons, was roughly evaluated to be $3.2 \cdot 10^{-16} cm^2$/bit in the case of a sensitive depth of 1 μm [11].

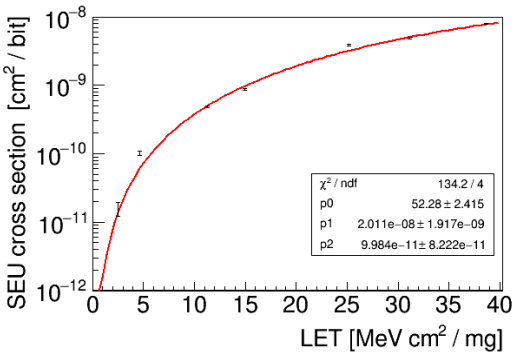

Figure 3: Cross section for upsets per bit of the PAStA chip

To obtain a direct measurements of upset numbers in the channel configuration registers of PAStA, a second test was performed with proton beams [12] at the experimental room of INFN-TIFPA in the proton-therapy Centre of Trento. The device is positioned in front of the beam line outlet and the proton flux on the device was obtained using wire chambers, with an estimated error of 10%.

The proton energy was set to 131.3 MeV and measurements were performed at three different beam current values corresponding to $2.2 \cdot 10^9$ proton/($cm^2 \cdot$ s), $4.4 \cdot 10^9$ proton/($cm^2 \cdot$ s) and $6.2 \cdot 10^9$ proton/($cm^2 \cdot$ s). No upsets were detected during tests with the first two proton beams. With the last one, upsets were detected and a cross section value of $3.5 \cdot 10^{-16} cm^2$/bit was estimated.

4. Conclusions

The radiation tolerance to upset effects of circuits implementing TMR and Hamming encoding techniques developed with a commercial 110 nm CMOS technology was investigated. The circuits under test are the channel configuration registers of PAStA, the custom readout circuit of silicon double-sided micro-strips of the PANDA MVD. The obtained result is adequate since the number of upsets expected in the micro-strip detector equipped with 3112 electronics readout chips, is less than 1 bit flip per hour taking into account that an evaluated particle flux of $5\cdot 10^4$ hadrons/cm^2 contribute to upset effects.

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