PROCEEDINGS OF SCIENCE

Integration, Commissioning and First Experience of ALICE ITS Control and Readout Electronics

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For the third running period of the CERN LHC, the ALICE experiment will undertake several upgrades of its sub-detectors. One of the detectors to be upgraded is the Inner Tracking System, featuring the new ALPIDE pixel chip. Control and readout of the 24120 chips are handled by 192 custom FPGA-based readout units. Each readout unit can forward 9.6 Gbps of data to another custom PCIe card that aggregates the data from several units and transmits it for further offline/online analysis. Integration and commissioning of the system is underway and this paper describes the first experiences and results of this effort.

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1. Introduction

During the ongoing Long Shutdown 2 of the CERN LHC, the ALICE experiment will replace the existing Inner Tracking System (ITS), which is based on silicon strip sensors, silicon drift sensors, and silicon hybrid pixel sensors, with a completely new detector based on Monolithic Active Pixel Sensor (MAPS) technology.

The upgrade is needed to provide a more precise and efficient vertex reconstruction, and low transverse momentum (p_{T}) tracking. This is achieved through the reduction of the material budget by a factor 4 compared to the current ITS, installation of a reduced diameter beam-pipe, allowing for the inner-most layer to be closer to the vertex, and also by providing a continuous readout to sample the full interaction rate [1].

The aim of the upgrade is to be able to handle 50 kHz Pb–Pb interaction rate and several kHz pp interaction rate. However, the current design is aimed at achieving double the rate for Pb–Pb and 1 MHz for pp.

1.1 ALICE ITS detector

The new ITS design [1], shown in Fig. 1, utilizes a custom-designed silicon MAPS chip called ALPIDE [4]. The chip has a size of $15 \times 30\,\mathrm{mm}^2$ and has a matrix of 512 by 1024 pixels, each with a size of $29 \times 27\,\mu\mathrm{m}^2$. The design utilizes an asynchronous sparsified digital readout and can be operated in either triggered acquisition mode or continuous acquisition mode. It has a control interface for configuration and trigger reception, a clock input and redistribution, a high speed data link, able to operate at up to 1200 Mbps, and a slower 4-bit bus used for communication between master and slave devices.

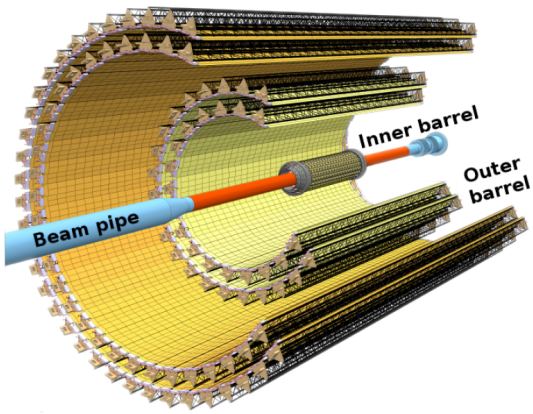

Figure 1: Upgraded ITS detector.

The 24120 ALPIDE pixel sensors are mounted onto 192 azimuthally overlapping staves arranged into seven coaxial cylinders of increasing diameters. The cylinders are separated into inner and outer barrels, consisting of three and four cylinders, respectively. Additionally, the outer barrel is separated into two middle layers and two outer layers, where the primary difference is the number of modules in the length direction.

Each stave in the inner barrel consists of nine ALPIDE chips, that are mounted onto a shared flexible-printed circuit board, providing the power, control, clocking and data for the devices. Each chip operates independently and has its own separate high-speed serial data output-link operating at 1200 Mbps. The clocking and control bus is shared among the devices.

The outer barrel uses modules consisting of two groups of sensors. In each group there is one chip assigned as the master chip and six chips that are slave chips. The master forwards the data from the six slaves over a 400 Mbps link, in addition it redistributes the clocking, control, and

triggering to the slaves. The staves consists of 2x4 and 2x7 of those modules, for the middle layers and outer layers, respectively.

1.2 Readout system

Trigger distribution, readout, control, power management, and monitoring (voltages, currents, and temperatures) of the sensors is handled by 192 custom Readout Units (RUs) based on a Xilinx UltraScale FPGA [2]. The Readout Electronics and the ALPIDE sensors can operate both in triggered and continuous readout mode. In continuous mode the RU internally generates periodic triggers to the sensors. Each RU, seen pictured in Fig. 2, is assigned to interface with only one stave. For the inner layers, nine high speed links running at 1200 Mbps connect the RU to the stave, for the middle and outer layers there are 16 and 28 links per stave, operating at 400 Mbps. The RU repacks the data from the sensors and forwards it over three optical transceivers, each supporting a maximum throughput of 3.2 Gbps, to a Common Readout Unit (CRU) [5] hosted in a commercial server, referred to as the First Level Processor (FLP). Each FLP will host up to two CRUs and each CRU will receive data from up to eight RUs. The CRU aggregates the data from the different links and forwards it over Ethernet to the Event Processing Node (EPN) for storage and further analysis. A schematic overview can be seen in Fig. 3.

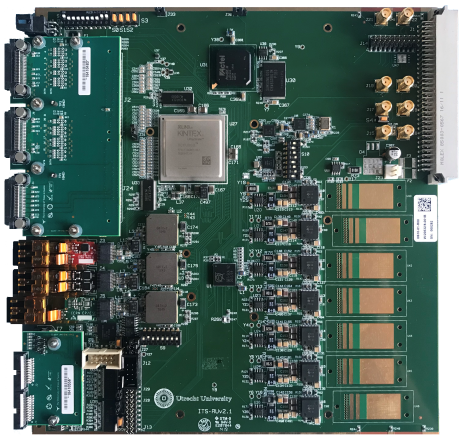

Figure 2: ITS Readout Unit.

Each RU receives the triggering information from the Central Trigger Processor (CTP), via a Local Triggering Unit (LTU), over a dedicated optical link. The RU also has the task of controlling and monitoring the Power Board (PB), a custom designed powering unit for the staves. Control of the RU is done from the Detector Control System (DCS) via one of the optical links connected to the CRU. A custom protocol allows for direct access to internal registers in the FPGA design, which enables configuration, control, and monitoring of the RU, sensors, and PB. For redundancy, this can also be accessed via a Controller Area Network (CAN) bus. An auxiliary FPGA, a Microsemi ProASIC3, is also present on the RU. It provides the initial configuration of the Ultrascale FPGA upon powerup, as well as doing scrubbing of the configuration memory of

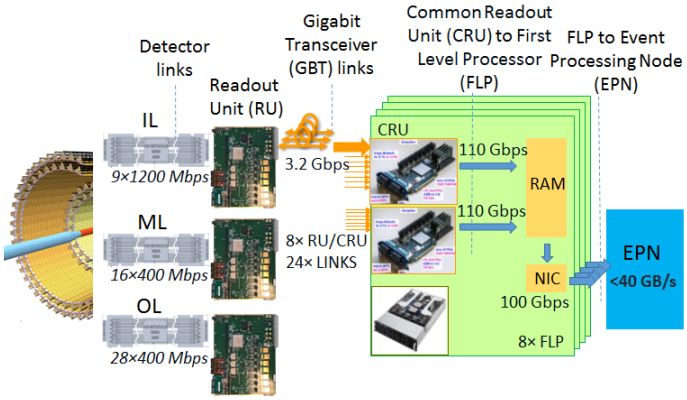

Figure 3: Bandwidths in the ITS data acquisition system.

the Ultrascale during operation, to correct any errors caused by radiation effects. A block diagram of the complete system is shown in Fig. 4.

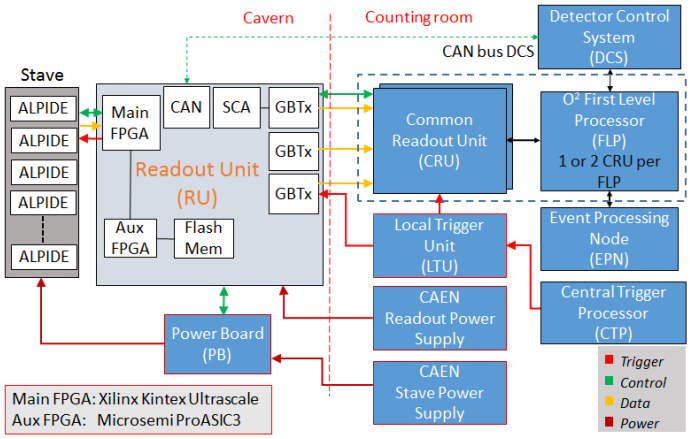

Figure 4: Block diagram of the ITS system.

2. Results

The ALPIDE chip uses a globally set charge threshold for discriminating pixel hits. Due to process variations, this threshold varies from chip to chip. The threshold is found by help of an internal test structure that can inject a known charge by using a capacitor and a Digital to Analogue Converter (DAC). By adjusting the charge and observing the number of times the pixel fires for a given charge, a probability s-curve can be fitted to the data. From this curve the thermal noise and the threshold can be found. [3]

Preliminary testing of the readout chain and tuning of thresholds has been done on one half inner layer, as can be seen in Fig. 5. The top left shows the result of finding the threshold for each pixel, the bottom left shows the thresholds after the front-end parameters have been tuned to achieve the best uniformity. The histogram on the right shows the threshold values pre- and post-tuning.

To verify the uniformity a test with an Sr90 source has been done. Figure 6 shows the data taken from this test. The uniformity is good and even detector structures can easily be seen, like the capacitors of the power distribution and the shadowing due to the slight overlap between staves.

3. Conclusion

The ALICE physics program requires a new, fast, low material budget, and radiation tolerant Si tracker. Because of this, the TowerJazz 180 nm CMOS technology was selected for the ALPIDE pixel sensor. Mass production and testing of the sensors have been completed. In addition, the stave production is nearing completion. Readout Unit and Power Board production is completed as well, and all the infrastructure for layer assembly, testing and commissioning is available. The commissioning is still ongoing and installation in the experiment is planned for summer 2020.

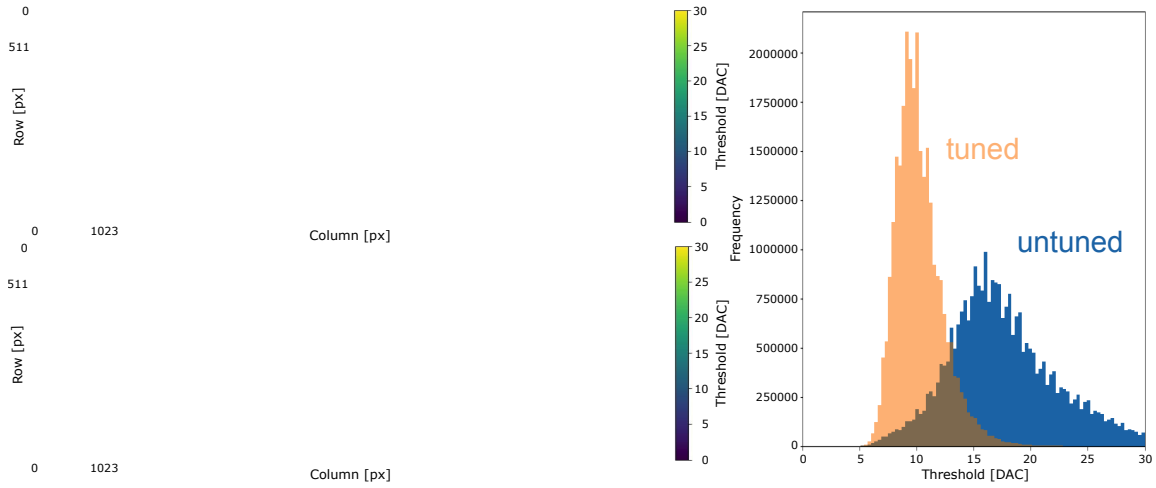

Figure 5: Threshold tuning for half-layer 0.

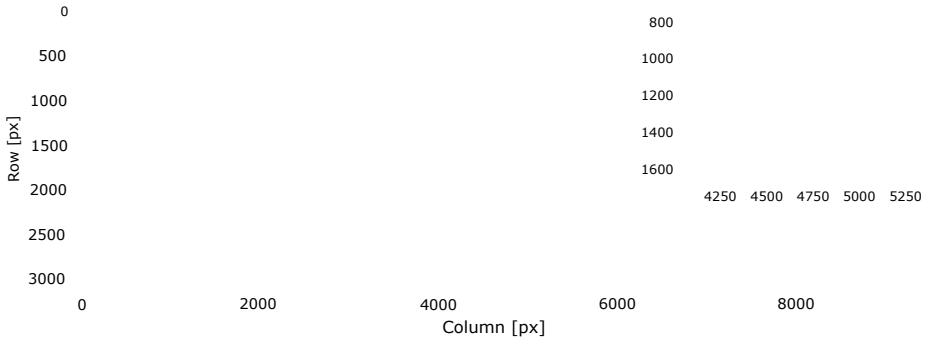

Figure 6: Test with Sr90 source.

References

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