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Test results of a Flexible Printed Circuit for the ATLAS High Granularity Timing Detector

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The compact structure of the HGTD proposed for the High Luminosity ATLAS detector upgrade at the CERN LHC requires a design to match the tight mechanical and electrical constraints. Our proposal based on a flexible printed circuit manages the signals to read out and control the modules, to bias the sensors with high voltage and to power the ASIC. Because of the high speed serial link, it is crucial to match the characteristic impedance of the lines. The high voltage bias requires clearance and shielding to limit the interference with the digital logic. We present results of the geometrical and electrical tests performed on the first version of the prototype.

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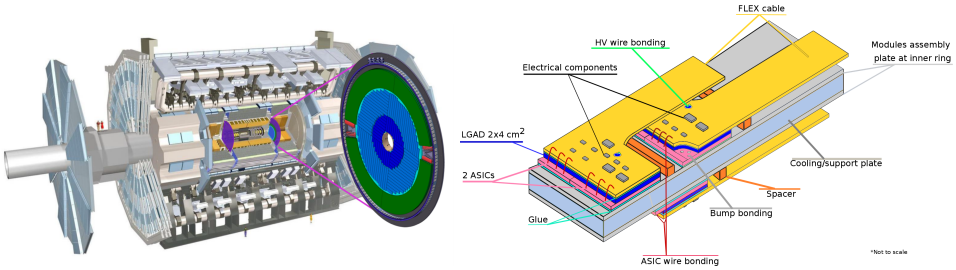
1. High Granularity Timing Detector

A High-Granularity Timing Detector (HGTD) is proposed for the Phase II upgrade of the ATLAS detector. The number of collisions per bunch crossing is increased at the High Luminosity LHC (HL-LHC) leading to a new challenge in the upgrade of the ATLAS detector. The HGTD will improve pile-up migation, as well as b-tagging and lepton isolation performance by providing precise timing information associated to each track in the endcap region (σ_t = 30 ps per track with $2.4 < |\eta| < 4.0$) [1]. The basic detector unit, so-called module, consists of a 2×4 cm^2 Low Gain Avalanche Detector (LGAD) [2] bump-bonded to two ASICs (2×2 cm^2 each). This element is glued and wire-bonded to a Flexible Printed Circuit (FLEX cable) connecting the electrical signals and supplying power between the module and the peripheral electronics The active area shown in Fig.1 is covered with modules placed on readout-rows, represented by the segmented regions. The most populated row consist of 19 modules (placed on the top and bottom sides of the cooling plate) and therefore, 19 FLEX cables.



(a) (b)

Figure 1: (a) Illustration of the HGTD, showing the peripheral on-detector electronics in green and the layout of the readout rows, containing modules mounted on half disk support plates (blue) [1]. (b) Schematic drawing of two adjancent modules on the top side and one of the bottom side of the support plate.

2. Flexible cable requirements and specifications

The FLEX cable, based on flexible printed circuit technology, connects the signals from the module to the peripheral on-detector electronics. The geometrical constraints are determined by the available space between two layers, the distance between the modules and the peripheral electronics and the maximum number of modules per readout row. Considering the requirements for the harshest constraints, the FLEX cables must have a maximum length of about 750 mm, width of less than 19 mm, and thickness of less than 350 µm. An L-shape was chosen as the baseline design with a width of 39.5 mm in the region to be glued to the bare module (18 mm length) and a 19 mm wide tail for the remaining length. The cables will be produced with different lengths and with the tail either on the right or on the left side of the module. In terms of electrical requirements, one HV line has been included in the design in order to bias the LGAD sensors at maximum 1 kV. The types of signals to and from the ASICs in each FLEX cable include differential pairs for the data transmission at 1.28 Gbit/s as well as clock and power signals. The signals for each module are listed in Tab. 1. The electrical requirements for the ASIC are two voltage supplies at (1.2 ± 0.2)V and the nominal impedance of the lines to be 100 $\Omega \pm 10\%$ for differential and 50 $\Omega \pm 10\%$ for

Table 1: Type and number of signal lines for one module included in the flex cable design.

Signal name	Signal type	No. of wires	Comments
HV	1 kV max.	1	Clearance
POWER	$1 \times$ Vdda, $1 \times$ Vddd, 1.2 V	2 planes	$R < 2.7\,\mathrm{m\Omega/cm}$
GROUND	Analog, Digital	1(2) plane(s)	Dedicated layer $R < 0.7\,\mathrm{m\Omega/cm}$
Slow control	Data, Ck (opt. + rst, error)	2 to 4	I^2C link
Input clocks	320 MHz, Fast command e-link (opt. 40 MHz (L1))	4 or 8	CERN Low Power Signalling (CLPS)
Data out lines	Readout data	4 pairs	4 e-links differential CLPS
ASIC reset	ASIC_rst	1	Digital
Monitoring	Temperature, Vdda, Vddd	6	DC voltage
Debugging	ASIC_debug	2	Analog

single-ended lines. The high-voltage to bias the sensor is expected to be in the range 600-1000 V. Finally, the same radiation tolerance is required as for sensors and ASICs, i.e. up to at least 4.7 MGy, as well as operation at a temperature of about $-30\,^{\circ}$C.

3. FLEX cable prototype

As part of the initial study phase, a prototype has been designed with the aim to understand the technology requirements (materials, manufacturing capability, electrical and mechanical robustness) and address any potential problems by representing a significant subset of the signals (signal integrity, power distribution, HV insulation, interference and crosstalk). 4 prototypes of 750 mm length, see Fig. 2, have been designed in the Detector Lab and manufactured at CERN PCB service. The stack-up of the cable is a 4 layer design. On the top layer the single lines are routed as micro-strips. The differential pairs as well as the HV line are placed in layer 3 as striplines in order to improve the impedance matching of these lines. Layers 2 and 4 are copper planes dedicated to power and ground. A polyimide film from UBE is the choice as dielectric material.

(a) (b) (c)

Figure 2: (a) FLEX cable prototype. (b) and (c) Extremities of the prototype.

4. FLEX cable testing

4.1 Power Integrity simulation and tests

A simulation of the voltage drop in each plane was performed with the Cadence Allegro Sigrity PI software package [3] and used to estimate the expected resistances of the planes. Table 2) shows

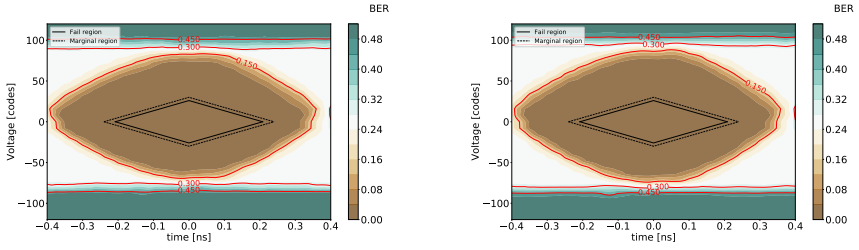
Table 2: Simulated and measured resistance of the analog and digital planes for the FLEX cable prototype.

Planes	Simulated resistance (mΩ)	Measured resistance (mΩ)
Analog	440	436±5
Digital	229	230±5

a comparison of these estimates with the FLEX cables. The analog plane shows a larger resistance than the digital one due to the different width chosen for the prototype design.

4.2 Signal transmission

To emulate the digital transmission from the ASIC an FPGA based on the Kintex KC705 evaluation board [4] has been programmed and connected to the FLEX cable via an adapter board to build an automatic test setup for all the types of cables that are under test. The FPGA injects test patterns at 1.25 Gbit/s and checks the response with the Integrated Bit Error Rate Test (IBERT). The SMA connectors placed on the adapter board are used to route the signals to the oscilloscope for classical eye-diagram analysis. A wire bond between two differential pairs at the end of the flex cable creates a loopback path for the signals. Therefore, the transmission length of the signals is twice the FLEX length, i.e. 150 cm. The test configuration and the I/O drivers are compatible with the VC707 FPGA [5] used by the LpGBT system [6]. In this way we assure the same conditions for the signal transmission as for the on-field operation. The IBERT detected no errors over a few days, yielding an upper limit at 95% confidence level (C.L.) on the error rate for one of the longest FLEX cables of 1.25 Gbit/s with a 95% C.L. BER limit of 10^{-15}. This value is well below the acceptable error rate of 10^{-12}. The same test was repeated with the HV up to 1000 V (1 mA) no error was detected for the same interval of time with a BER result about 10^{-15}. The Kintex KC705 evaluation board encodes the signals at the receiver side after an equalization stage. The signals were measured prior to the equalizer by an oscilloscope. The signal amplitude ranges from ±100mV to ±200mV. The eye diagrams in Fig. 3 measured without HV (a) and with HV (b) show a similar shape and opening area. The opening areas for both eye diagrams are much larger than the no-error-accepted area indicated by the mask.

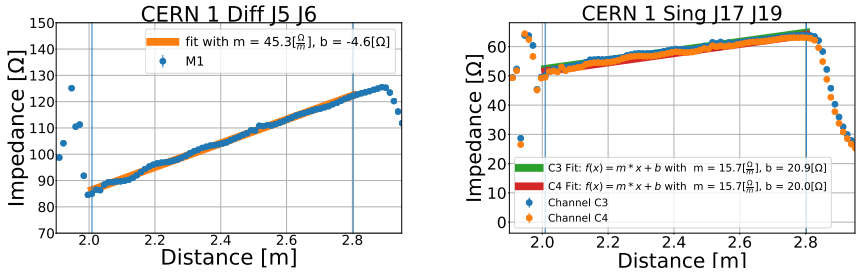


(a) (b)

Figure 3: Eye diagrams for the FLEX cable prototype. (a) HV = 0V (b) HV = 1000 V. The solid line indicated the mask in which no errors are acceptable, the dashed line is the marginal region in which few errors can be tolerated according to Kintex.

4.3 Impedance control: Time Domain Reflectrometry measurements

The Time Domain Reflectrometry (TDR) measurement is performed in order to check the impedance homogeneity of the tracks, which is crucial for high-speed data transmission. Two assembled flex cables were used to measure two differential pairs and two single lines that are accessible from the adapter board. The TDR module 80E08 together with the DSA8200 oscilloscope by Tektronix [7] was connected through SMA connectors to the adapter board. All the differential pairs and single lines were measured and compared with the nominal value mentioned above as shown in Fig. 4.The values exhibit a linear behaviour since the copper track is a lossy line and resistive effects are playing a role. This behaviour will be further investigated with the manufacturer to adapt the design accordingly.



(a) (b)

Figure 4: Results of the differential impedance for a differential line (a) and the impedance for a single line (b) in the FLEX cable. The vertical lines indicate the region of the flex cable. The orange line in (a) and the green and the red lines in (b) correspond to the impedance measurement fit for two single lines of and for a differential pair. The uncertainties parameters are about 0.3 for the slopes, m, and 0.8 the offsets, b.

5. Summary and outlook

A first prototype of the FLEX cable for the ATLAS HGTD has been tested. The first results show an agreement with the requirements in terms of signal transmission. The behaviour of the impedance measurements on the tracks will be followed up with the manufacturer. Further tests are planned in order to study the performance of the prototype at operational conditions such as the signal transmission at $-30\,^{\circ}$C as well as tests to measure the jitter and the crosstalk. Additionally, tests to measure the voltage drop and the LV influence on the HV are also planned.

References

[1] *HGTD Technical Proposal, LHCC-P-012*, CERN-LHCC-2018-023, July 2018

[2] N. Cartiglia et al., Performance of Ultra-Fast Silicon Detectors, JINST 9 (2014)

[3] Cadence Sigrity and PowerSI Cadence Design Systems Inc.

[4] KC705 Evaluation Board. Xilinx Inc.

[5] VC707 Evaluation Board. Xilinx Inc.

[6] LpGBT project. GBT project "Radiation Hard Optical Link Project"

[7] DSA 8200 Digital Serial Analyzer Sampling Oscilloscope. Tektronix