

First results from the CIC data aggregation ASIC for the Phase 2 CMS Outer Tracker

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The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase 2 CMS Outer Tracker at the High-Luminosity LHC (HL-LHC). Prototyped in a 65 nm CMOS technology, the CIC aggregates the digital data coming from eight upstream front-end chips, formatting it into data packets containing the trigger information from eight bunch crossings and the raw data from events passing the Level 1 (L1) trigger, before transmission to the lpGBT. The role of the CIC in the readout chain is to provide an extra factor of data reduction by grouping data over time and space. A first prototype, the CIC1, integrating all functionalities for system level operation, has been tested in early 2019. A brief description of the functionalities and the test results obtained concerning the performance characterization and the radiation tolerance of the chip are presented in this contribution.

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1. Introduction

For the Phase 2 upgrade of the High-Luminosity LHC (HL-LHC), the CMS experiment needs a completely new silicon Outer Tracker (OT) detector able to cope with high pile-up conditions and withstand significantly higher radiation fluences. The future OT will be populated with two types of module, each one based on paired silicon sensors: the Pixel-Strip sensor pairs (PS modules) located in the innermost region of the OT tracker and the Strip-Strip sensor pairs (2S modules) in the outer part [1].

The *Concentrator Integrated Circuit ASIC* (CIC) equips the Front-End Hybrids (FEH) of the modules and it is the only shared component between the two different type of FEH. The CIC role in the readout chain is to collect the digital data coming from 8 upstream FE chips (MPAs [2] in the case of PS, CBCs [3] in the case of 2S) and buffer, aggregate and format them into output packets to be transmitted to off-detector readout electronics, via the LpGBT and VTRX+ optical link. Two data streams are generated by the FE chips and are managed by the CIC. The first one, called the *Trigger data* stream, contains information necessary for the L1 trigger processing electronics to form a trigger decision. This information is collected by the CIC from 8 FE chips over eight 25 ns bunch crossings (BX), and is reconstructed and filtered to form a data packet that is sent synchronously over 8 periods of the 40 MHz clock through the 6-bit wide trigger output bus. The hit data from events passing the L1 trigger, buffered by the 8 FE chips, constitutes the second data stream called *L1 data*: it is transmitted by the CIC asynchronously, upon reception of the L1-accept signal. Figure 2 represents the block diagram of CIC functionalities. Two CICs will be used per module, for a total number of approximately 26600 in the whole Outer Tracker. Due to the different power distribution networks between PS and 2S modules, the digital core of the CIC has been designed to work at 1V (in the case of PS) and 1.25V (in the case of 2S), while the custom SLVS drivers and receivers are powered at 1.25 V in both cases. More details of the CIC architecture and design can be found in [4].

The first silicon version of the CIC architecture (CIC1) has been tested with a standalone testbench using test patterns emulating both flavours of the modules. A second real-world system capable of stimulating all the FEs of a prototype 2S module has been also used.

2. Functional tests

The CIC1 is a 2.8×6.5 mm bump-bonded flip-chip but for ease of testing the first prototype has been fabricated for a wire-bond process. All the tests have been performed on chips wire bonded on passive carrier boards in order to facilitate the characterization and the tests. Figure 1 shows the standalone custom test setup based on three boards. The passive carrier board is plugged on a custom interface board for voltage level translation, power regulation, addition of delays on data input lines and monitoring purposes. Firmware and software routines based on the standalone verification testbench used to model the ASIC design have been developed to run on a Xilinx KCU105 development card, connected to the custom interface board. The test routine to perform functional tests consists of generating synthetic data with CMS simulations to emulate the outputs of the 8 FE ASICs. A software simulation of the ideal model uses such data to emulate the expected CIC1 outputs. The FE data are stored in the KCU105 RAM and sent to the CIC1: the RAM data capacity allows the possibility to test the CIC1 for

tens of millions of consecutives BXs. The CIC1 output packets are then recorded in the RAM and compared in software with the expected values, previously obtained by the software simulator. All the CIC1 functionalities, starting with the startup sequence based on the hard reset deassertion and I2C configuration have been successfully tested following the previously described routine. Since the CIC1 input data are produced by 8 different FE ASICs, each one clocked by a common external 320 MHz clock, a bitline phase alignment feature is required in order to resynchronize the phase of the 6x8 CIC1 input lines, using the internal system clock. This feature allows the CIC1 to automatically delay the phase of each input line when a repetitive pattern is presented or to apply a fixed delay configuration to the input lines when the input phases are already known. Moreover, the word alignment feature that allows the CIC1 to correctly reconstruct the input data words with respect to the 40 MHz internal clock was positively validated, along with the ability to correctly detect the first event frame after the issuing of a resync command (BX0 detection). The test procedure validation included the verification of data output transmission for 4 different modes (PS and 2S for both L1 and Trigger data output). Further tests demonstrated that the CIC design is robust against various error configurations of input data. This includes tests with single bit flips in the data frame and validation of chip behavior after an orbit reset.

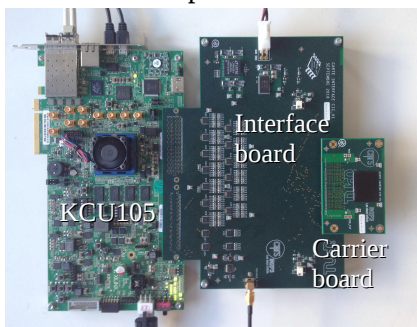


Figure 1: CIC test setup.

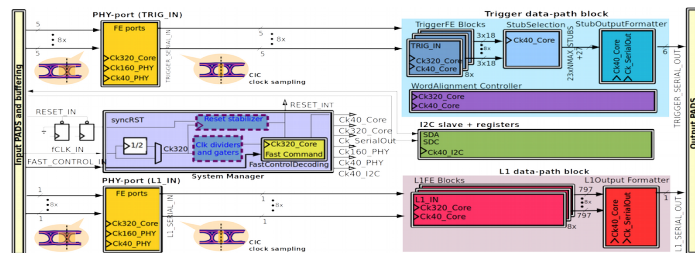


Figure 2: CIC block diagram.

Power consumption measurements were performed during 5 different CIC1 running windows at 5 different core voltages. Figure 3 shows the overall power consumption of the CIC1 during all calibration and processing steps where the core and the periphery of the chip are powered at 1.2V. The maximum power consumption is reached during the phase alignment step (240 mW) which only occurs during chip initialization, while the typical power consumption (210 mW) is achieved during the data sending phase. In Figure 4, the peaks correspond to the extraction of 10 L1 events after the acceptance of 10 random L1 triggers. The design complies with the allocated power budget (250 mW in PS mode; 312.5 mW in 2S mode) even if no power consumption optimization techniques have been applied to the first CIC prototype.

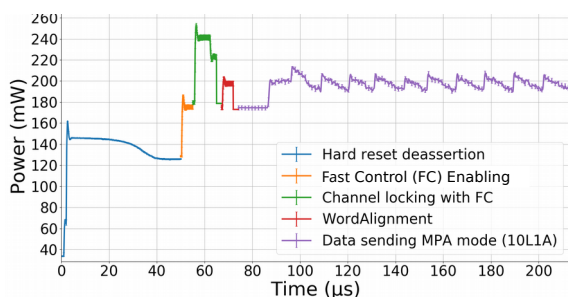


Figure 3: Power consumption measurements during CIC calibration and processing steps.

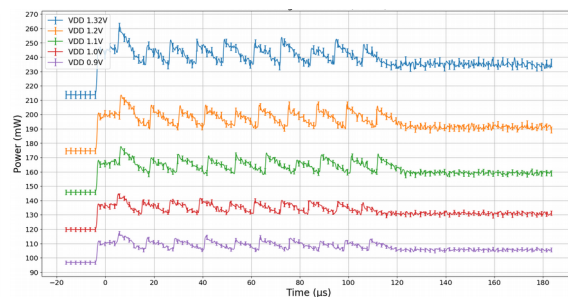


Figure 4: Power consumption at various core voltages, during transmission of 10 L1 data frames (MPA mode).

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3. Real-world test

The CIC1 has also been tested with a prototype 2S hybrid containing 8 FE chips (CBC3.1) [5]. It's the first real-world test of the CIC1 within a FEH with the aim of validating the complete readout chain. The OT- μ DTC (micro Data, Trigger and Control) test system is based on the μ TCA FC7 data acquisition and control card, built around a Kintex7 FPGA. Figure 5 shows the 2S electrical characterization board used for the translation and buffering of the CIC1 output lines, which accommodates the 2S prototype hybrid with 8 CBC3.1 and a CIC1 mezzanine. This characterization board is connected to an FC7 [6] where a dedicated firmware for complete hybrid readout and control is implemented.

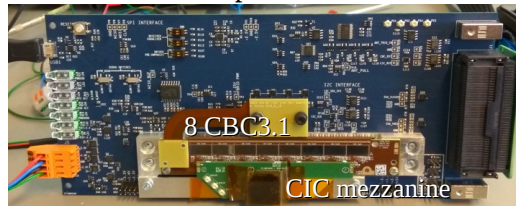


Figure 5: 2S electrical characterization board with 8 CBC3.1 and 1 CIC mezzanine on a prototype FEH.

The tests performed with the OT- μ DTC system have verified the communication between the different components of the set-up and the consistency of the CIC1 output with respect to what is expected from CBC3.1 under different conditions. Such tests also validated the ability for the CBC3.1 to generate the phase and word alignment patterns required for the CIC1 initialization and the correct operation of the CIC1 automatic phase-locking feature. The effectiveness of the automated BX0 identification procedure of the CIC1 is also confirmed.

4. Total Ionizing Dose irradiation tests

The Total Ionizing Dose (TID) sensitivity of the ASIC has to be tested due to the extreme radiation environment expected at HL-LHC. The CIC1 was irradiated up to 210 Mrad in an X-ray beam over a period of 24 hours. The total dose attained is well above the 100 Mrad maximum expected for the HL-LHC. The CIC1 was standalone tested in the beam and stimulated with patterns emulating trigger and L1 data from the CBC, generated by the OT- μ DTC. The test routine firstly performs phase, word and BX0 alignment of the CIC1 as if a CBC is connected and saves the results of the optimal input locking phases, word and BX0 alignment. After this initialization phase, CBC trigger data (~ 1500 consecutive BXs, issued from the validation framework) are sent to the CIC1 and the packaged trigger data are saved for later comparison to the validation framework. Two different CBC trigger data files were used, always alternating between both. The routine of phase, word and BX0 alignment followed by data playing was repeated throughout the irradiation. Power supply currents on the periphery (I_{PST}) and core (I_{core}) along with the temperature (Figure 6) were monitored during the entire procedure. Figure 7 depicts a decrease of ~ 1.5 mA after 200 Mrad on both currents. A further decrease of ~ 2 mA on I_{core} after 10 hours of annealing was observed. The pre-irradiation (pre-rad) average value of I_{core} is 192 mA, while for I_{PST} is 22.7 mA. Temperature dependent pre-rad studies observed that the rise in I_{core} at the start of irradiation and the drop post-rad can only partly be attributed to the temperature variations. The start-up sequence and data integrity were validated after irradiation. The validation included the correct locking of phase alignment on all

data lines, word alignment on all trigger data lines and BX0 alignment (each loop reports the same time difference in BX units with respect to the Reset-sync signal). Moreover, no radiation dependent upsets in either of the data streams were observed.

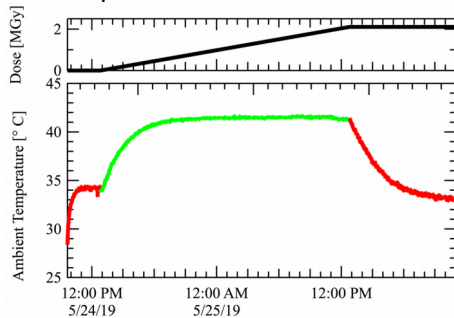


Figure 6: Trend of the temperature during the TID test (probe right next to the CIC1).

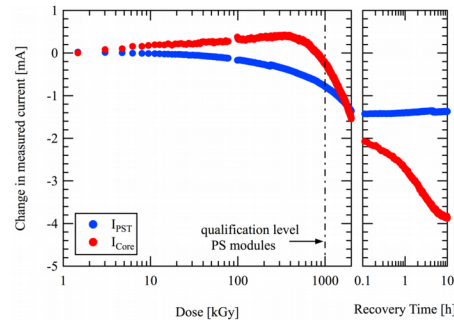


Figure 7: Measured I_{core} and I_{PST} during the irradiation.

5. Conclusions

The first prototype of the CIC architecture has been realized in a commercial 65 nm CMOS technology and its tests started in early 2019. Functional tests on the standalone chip and within a complete data acquisition chain validated all its functionalities. Two testbenches have been designed for performing the tests. The measured power consumption is lower than 250 mW which meets the specifications for the CMS OT. The TID tests validated the integrity of the data and no errors were observed during or after the irradiation. A new version of the CIC architecture has been submitted to the foundry in July 2019 including triple module redundancy techniques in order to obtain the required Single Event Upset (SEU) resistance of the architecture. The design has also been optimized to further reduce the power consumption.

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