PROCEEDINGS OF SCIENCE

Production and Quality Control of VFAT3 Front-end Hybrids for the CMS GE1/1 Upgrade

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The CMS experiment is planning to install Gaseous Electron Multiplier (GEM) chambers as part of the Muon upgrade for High Luminosity Operation at the LHC. The front-end ASIC (VFAT3) has been produced in volume together with its hybrid PCB. This paper describes the design of a custom test bench for the production Quality Control (QC) of the VFAT3 hybrids. The full QC procedure incorporates calibration and performance measurements, database entries and statistical data analysis. The paper details the firmware and software functions to achieve the test time per hybrid to 2 minutes. The test system produced an overall 89% production yield including the wafer dicing and hybrid assembly losses.

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1. Introduction

The Large Hadron Collider (LHC) will be upgraded in several phases to expand its physics program significantly. After the long shutdown of 2019 and 2020 (LS2) the accelerator luminosity will be increased to $2 \cdot 3 \times 10^{34} cm^{-2} s^{-1}$ exceeding the design value of $1 \times 10^{34} cm^{-2} s^{-1}$ allowing the CMS experiment to collect approximately 100 fb^{-1} per year. A subsequent upgrade in 2022-23 will increase the luminosity up to $5 \times 10^{34} cm^{-2} s^{-1}$. The CMS muon system must be able to sustain a physics program after the LS2 shutdown that maintains sensitivity to electro-weak scale physics and for TeV scale searches similar to what was achieved up to now [2]. To cope with the corresponding increase in background rates and trigger requirements, the installation of additional sets of muon detectors, referred to as GE1/1, GE2/1, and ME0 that use Triple-GEM (Gas Electron Multiplier) technology has been planned. The installation and commissioning of the GE1/1 chambers are ongoing now and will continue through 2019 and 2020, while the GE2/1 and ME0 detectors are expected to be installed after 2022. The front-end ASIC (VFAT3) has been produced in volume together with its hybrid PCB. VFAT3 is a 128 channel custom ASIC designed explicitly for the readout of GEM detectors for this high luminosity upgrade of the LHC (HL-LHC).

2. VFAT3 Architecture and Hybrid PCB

Each VFAT3 front-end channel consists of a pre-amplifier, a shaper, a single-to-differential, and a Constant Fraction Discriminator (CFD) stage, as shown in figure 1. The CFD converts the analog signal to real-time binary "hit " information based on the applied threshold. The "hit" information is separated into two distinct paths. The first is the trigger path, which provides binary "hit" information in real-time with a fixed latency [1]. CMS uses this information for trigger building. The second is the tracking data-path, which provides data packets following receipt of a trigger and contains full granularity "hit" information plus time stamps and status flags. VFAT3 also has built-in Calibration, Bias, and Monitoring(CBM) circuitry to internally inject known charge pulses to all the channels to compute the front-end noise floor and thresholds [3].

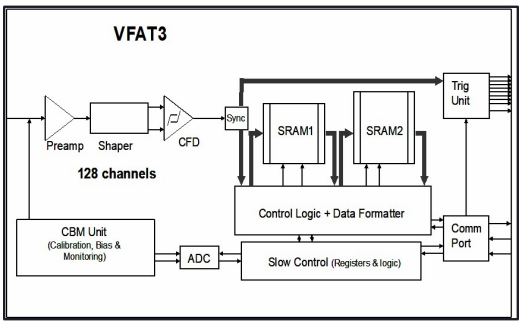

Figure 1: VFAT3 ASIC block diagram

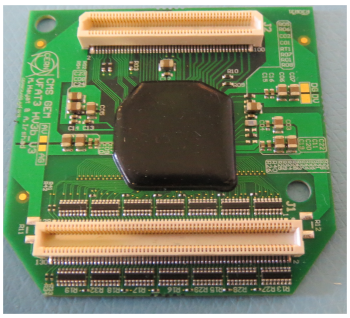

Figure 2: VFAT3 HV3B_V3 production hybrid

For GE1/1, the VFAT3 die is directly mounted as a chip-on-board device on the hybrid PCB which measures $43.5 \times 46.5 mm^2$. A series resistor of 470Ω is added at the input of each analog channel to achieve the robust protection against GEM discharges as shown in the figure 2.

3. VFAT3 Hybrid Test System

A VFAT3 hybrid test system is designed to characterize and qualify 5000 of the VFAT3 hybrids for GE1/1 GEM stations. The test system evaluates the noise levels of all VFAT3 front-end channels by using internal injection pulses of varying amplitudes. The test system consists of a Kintex-7 evaluation board, a custom verification board, a handheld infra-red temperature gun, a bar-code scanner, a programmable power supply, and a Linux PC with custom software. The firmware is based on a System-on-Chip (SoC) architecture with a microblaze processor connected to the Verilog HDL peripherals within the FPGA through Advanced Extensible Interface (AXI) bus architecture as shown in figure 3.

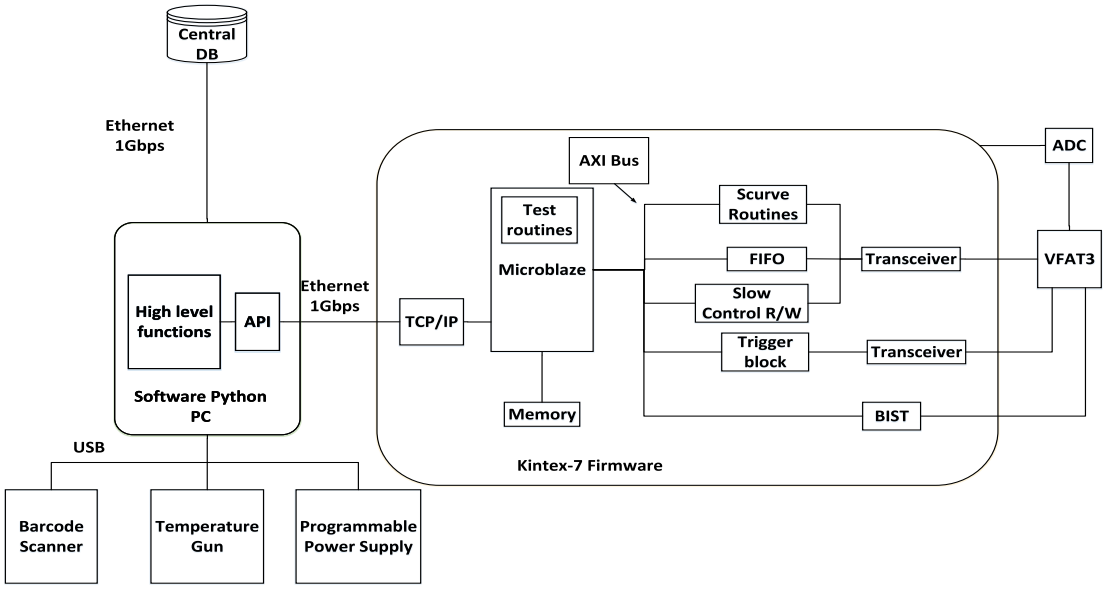

Figure 3: Production test system block diagram

The 320 Mbps serial data to/from VFAT3 is converted to the 40MHz clock domain in "Transceiver" blocks. The slow control data is parsed in the "Slow Control R/W" block, which consists of IP-Bus and HDLC sub-blocks. The tracking channel data is transferred to the "Scurve Routines" block, which parses data packets to extract channel hit information. The processed data is then transferred to microblaze which then re-transmits this data to the Linux PC through 1Gbps link.
VFAT3 also has a built-in temperature sensor that would be used to acquire a full GEM system temperature map during CMS operational runs. The offset correction of each sensor is required to compensate response variation in these sensors. An infrared temperature gun is used to measure the temperature of each hybrid during production and corresponding sensor offset.

4. VFAT3 Hybrid Test Flow

The Hybrid test flow is shown in figure 4. Every hybrid is visually inspected, and a barcode label is attached to it before the production test. The first system test looks for fatal functional issues and identifies the faulty hybrids at an early stage.

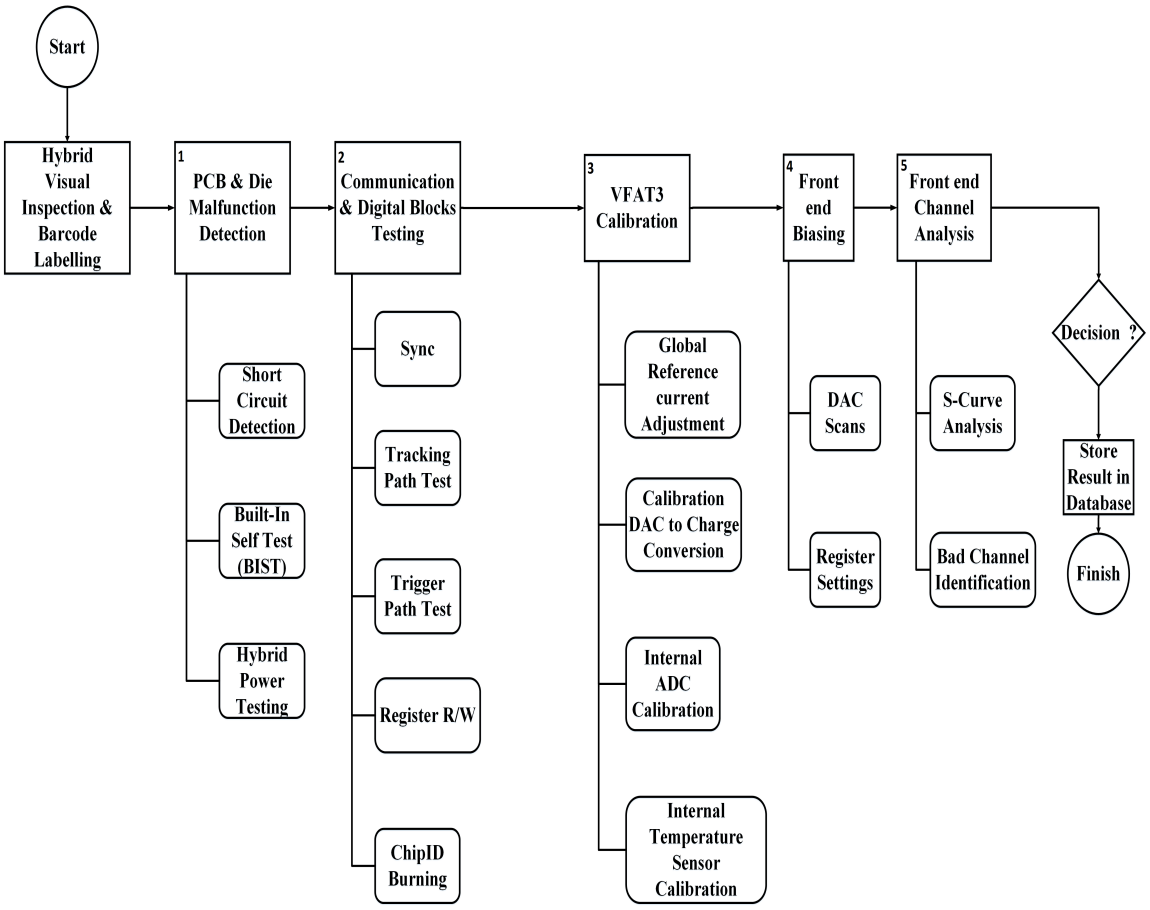

Figure 4: Production test flow diagram

In the second step, VFAT3 digital communication ports and all the digital functionality is verified. In the third step, the chip calibration is performed, and corresponding coefficients are computed. The DAC scans testing is performed to create lookup tables of DAC results that are used for front end biasing and calibration. In the fifth step, the front end analysis is performed to identify dead channels and compute the Equivalent Noise Charge (ENC) and channel threshold spread of all input channels of the chip. Finally, the production data and calibration coefficients are stored in the VFAT3 database.

5. Hybrid Production Statistics

The production of the VFAT3 hybrid was split up into smaller batches to facilitate fabrication and wire bonding steps. An overall production yield of 89% is achieved, as shown in figure 5. The 11% of the hybrids get rejected by the production test system, and a detailed breakdown of these rejected hybrids is also shown in figure 6. This bar graph shows the relative percentage of the different kinds of problematic hybrids that were rejected during production. Internal ADC issues, broken Memories, dead channels, and hybrid short were the four frequent issues found during the whole production. VFAT3 is wire bonded to the hybrid PCB, and many of the faults encountered during

the production tests may be correlated to bonding imperfections. Dead Analog channels mainly occurred due to missing bonds, and short-circuit reflects shorts between neighboring bonds. VFAT3 yield issue may also contribute to broken memories, broken ADC and noisy Analog channels.

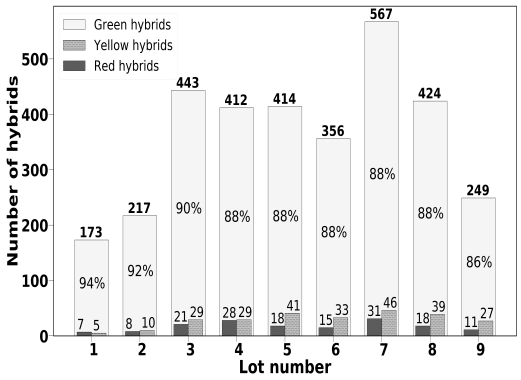

Figure 5: A bar graph showing VFAT3 hybrid production yield

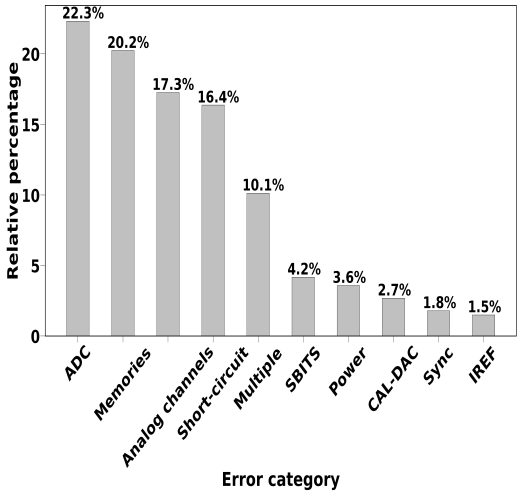

Figure 6: Relative percentage of rejected hybrids

6. Summary

A production test bench is designed to characterize and qualify 5000 of the VFAT3 hybrids for GE1/1 GEM stations. The test bench evaluates the noise levels of all VFAT3 front-end channels by using internal injection pulses of varying amplitudes. The test system also checks thoroughly every internal analog and the digital block of the chip. The speed of the production test is optimized for 2 minutes per hybrid. The overall production yield of 89% is achieved including die and hybrid assembly losses.

References

[1] P. Aspell et al. "VFAT3: A Trigger and Tracking Front-end ASIC for the Binary Readout of Gaseous and Silicon Sensors". In: *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*. Nov. 2018, pp. 1–8. DOI: 10.1109/NSSMIC.2018.8824655.

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[3] F. Licciulli et al. "Calibration, bias and monitoring system for the VFAT3 ASIC of the CMS GEM detector". In: *2017 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*. June 2017, pp. 81–84. DOI: 10.1109/IWASI.2017.7974222.