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Powering of the CMS Phase-2 Upgraded Tracker

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The LHC machine will be upgraded to increase its peak luminosity and targeting an integrated luminosity of 3000 to 4500 fb^{-1} in 10 years. The CMS experiment will be upgraded to meet new challenges such as unprecedented radiation environment, demanding high resilience, and increased number of events per bunch crossing, requiring higher detector granularity. Consequently, both the Outer Tracker (OT) and Inner Tracker (IT) will have to fulfill very stringent requirements also in the power distribution to the front-end electronics: the OT (more than 13000 independent modules) will use in situ DC/DC converters to parallel distribute 100 kW of power, while the IT will use a serial powering scheme to provide about 50 kW to thousands of modular units.

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1. Introduction

The Large Hadron Collider is going to be upgraded, targeting a peak luminosity of 5 to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [1]. Concurrently the CMS (Compact Muon Solenoid) experiment needs to upgrade its own apparatus, increasing the radiation resilience and the granularity of the detectors. A completely new system of central tracking silicon detectors is being designed [2], composed of innovative pixel detectors in the inner region (Inner Tracker) and silicon strip and macro-pixel detectors in the outer region (Outer Tracker). Two different powering schemes are used to provide bias to the sensors and low voltage power to the front-end electronics, for a total power consumption exceeding 100 kW for the Outer Tracker and 50 kW for the Inner Tracker. The two powering schemes and the status of their development are reported in this paper.

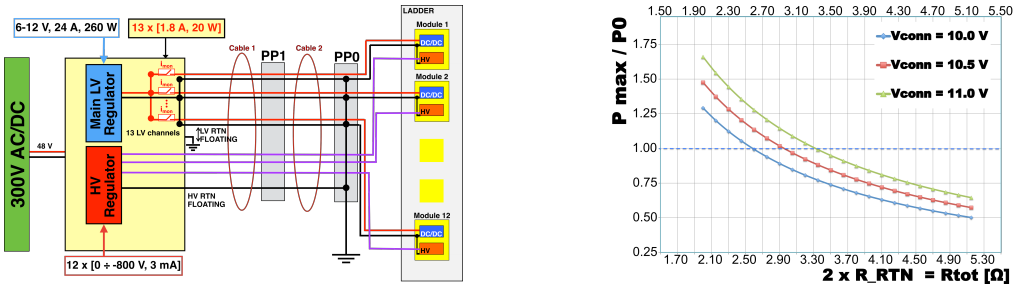
2. Outer Tracker Powering

The OT is made of more than 13000 modules, with a pair of sensors each, for a total amount of $\sim 42 \times 10^6$ strips and $\sim 170 \times 10^6$ macro-pixels. The total power required by the front-end electronics (FE) of each PS module (featuring one macro-pixel sensor and one strip sensor) is ~ 8.8 W, while each 2S module (featuring two strip sensors) requires ~ 5.2 W. The total power required by the OT exceeds 100 kW.

Modules can be operated independently and each of them receives one low voltage (LV) and one high voltage (HV) line. One of the requirements for the OT is to keep the material budget inside the tracking volume low. Bulky conductors, thus, cannot be used to bring LV to the modules, preventing the possibility of providing the required voltages directly from a remote power supply system. This scheme, in fact, would require three (two) distinct voltage lines per PS (2S) module, with severe voltage drops along the cables, which would imply huge power loss and the need to implement a very complex and fast remote sensing system in order to compensate the voltage drops and ensure the correct voltages at the detector. The chosen solution is to provide just one voltage line at 6 to 11 V per module, and to generate the required voltages in situ, using several DC/DC converters in a cascade configuration. The power distribution scheme on the modules, obtained using bPOL12V [3] and bPOL2V5 [4] DC/DC converters, is shown in Fig. 1. The power

Figure 1: Power distribution scheme for outer tracker: PS on the left, 2S on the right.

distribution is organized with a modularity of 12 channels (Fig. 2(a)), with one main regulator that provides the voltage (6 to 12 V) in parallel to them. Each channel is operated (on/off status) and monitored (current monitor with over-current safety) individually. In order to minimize the LV line resistance, the power cables are divided into three interconnected branches (Fig. 2(a)). From the PSM (power supply module) a ~ 60 m long cable with ~ 14.5 mm diameter reaches the "patch panel 1" (PP1) area located inside the electromagnetic calorimeter volume, in the barrel-endcap



(a) (b)

Figure 2: (a) Power group scheme. (b) Maximum disposable power as a function of total cable resistance for different values of maximum voltage at the power supply connector (V_{conn}), $P_0 = 8.8\,\mathrm{W}$ is the nominal power required by one PS module.

interface region. There a $\sim 6\,\mathrm{m}$ long cable (max. 10 mm diameter) is interconnected, reaching the "patch panel 0" (PP0) area located on top of the OT endcap-barrel interface region, just outside the tracking volume. At PP0 the cables are connected to the modules via individual Copper Cladded Aluminum (CCA) wires (gauge AWG24) partially bundled together ("octopus") and via a final "pigtail" connection made with AWG26 gauge CCA wires, covering a distance of $\sim 1.2\,\mathrm{m}$. In the PSM-PP1 branch for the LV lines, enamelled Cu conductors are used, alternating positive and return lines in a low-impedance configuration; in the PP1-PP0 branch AWG22 gauge Cu conductors are used. All conductors inside the tracking volume are made in CCA, thus keeping the material budget low. Thanks to this configuration the total resistive LV path between PSM and modules is below $1.3\,\Omega$. The total cable resistance is, indeed, one of the main factors limiting the maximum disposable power (P_{max}) to the modules. Figure 2(b) shows the ratio P_{max}/P_0 as a function of total cable resistance for different values of maximum voltage at the power supply connector (V_{conn}), where P_0 is 8.8 W. From this evaluation it emerges that with $R_{tot} = 2.6\,\Omega$ it is possible to provide the required power (without any margin) when $V_{conn} = 10\,\mathrm{V}$, while a possible 25% additional power is reachable with $V_{conn} = 11\,\mathrm{V}$.

Finally power system tests aiming to perfect the power system specification are ongoing. Thanks to these tests the enable circuit scheme has been already established. The bPOL12V DC/DC converters, indeed, require an enable signal to switch on and, in addition, they have an input under-voltage lockout threshold with hysteresis between switch on and off. The enable signal is provided by a voltage divider at the input voltage of the DC/DC converter. Hysteresis and voltage divider configurations have been established via tests performed using the FEAST_MP [5] (made in the "parent" technology of the bPOL12V), and validated by tests performed in Aachen with FEAST2 chips operated on prototype power hybrids [6]. Further tests were performed to verify that the system will not suffer from an oscillatory behaviour at turn on or turn off, with voltages at the DC/DC input crossing the enable and disable thresholds due to the voltage drops across the lines. The tests were performed as a function of the voltage ramp speed, cable resistance and DC/DC enable/disable thresholds. The configuration established avoids this kind of behaviour, identifying a proper operation range with ramp time values between 50 and 500 µs. Further tests were performed to confirm that abrupt current load variations in one module (up to 2 A) will not affect the voltage regulation to the front-end (FE) electronics inside the other modules connected to the same PSM.

3. Inner Tracker Powering

The IT consists of $\sim 2 \times 10^9$ pixels arranged in arrays and grouped in modules with 1×2 or 2×2 readout chips , for a total of $\sim$ 3900 modules requiring $\sim$ 50 kW. Optoelectronic services are detached from the modules and hosted on dedicated boards (portcards) located at the periphery of the detector, which are powered adopting a scheme similar to the OT one, based on DC/DC converters. DC/DC converters cannot be used in the detector modules region, since they cannot sustain the implied radiation levels and would require too much space and add considerably to the material budget in this region. Thus, the serial powering is the unique scheme compatible with the HL-LHC physics requirements. It makes use of a current source that provides a constant current to all the modules in a serially powered chain. It is a major technological challenge since it has never been used on such large scale. Thanks to the serial distribution scheme, as shown in Fig. 3,

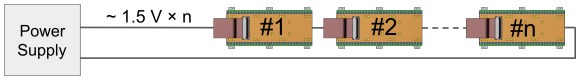
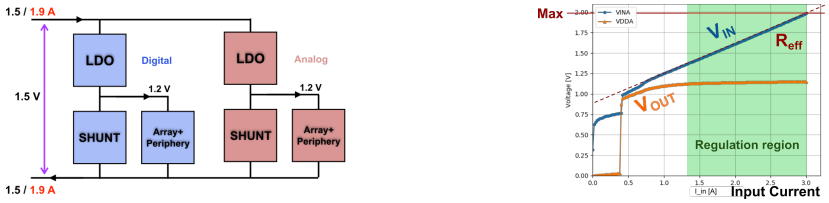


Figure 3: Serial powering concept.

the LV power is intrinsically distributed at the power supply output with voltages higher than the single module needs. This allows a huge reduction of power loss in the cables and stable voltage regulation in presence of variable loads. In order to power the full IT, $\sim$ 500 serial chains, with up to 12 modules, are needed, subdivided into 4 A chains, for 2-chips modules, and 8 A chains, for 4-chips modules. The readout chips (ROC) inside each module share the current in parallel. Also inside the chip the power is shared in parallel, between the analog and digital part. All the detector modules in a chain see the same current by construction, while the voltage can be equally shared only when all the detector modules constitute the same load. The Shunt-LDO (SLDO) IP



(a) (b)

Figure 4: (a) SLDO model. (b) Output and input voltages of the SLDO as a function of the input current.

block of the ROC (Fig. 4(a)) is responsible for ensuring the delivery of the correct voltage to the chip electronics (LDO functionality, Fig. 4(b) yellow line) and for isolating the chip power demand from the total current in the serial chain (SHUNT functionality). It is electrically equivalent to a resistor in series with a voltage source, $\Delta V = f(I)$ (V_{IN} in Fig. 4(b), blue line).

The RD53 Collaboration is developing the ROC for both ATLAS and CMS collaborations and the first prototype is the RD53A chip [7]. The chip has been extensively tested and laboratory tests and simulations are still ongoing. The serial powering concept has been established and serial chains with up to 16 RD53A chips were operated in the laboratory.

Concerning the HV distribution, the baseline foresees that the bias is distributed in parallel to the modules belonging to the same serial chain using a single voltage regulator. Extra care needs to

be taken considering LV and HV inter-operations. While a state with LV being off and HV being on must be forbidden, the HV generator circuitry must prevent sensor forward biasing when LV is on and HV is off. Referring to Fig. 5, each module has a "local reference" (V_{LR}) given by the lower

Figure 5: Forward bias behaviour with respect to power supply off mode.

voltage of LV that depends on the position of the module in the chain. The HV is distributed in parallel to the modules in the chain (V_{HV}), but the bias to the sensor is $V_{HV} - V_{LR}$, thus different for each of them. When the HV is off, the bias may not be 0 V and sensors can be slightly polarised, producing currents in the upstream circuit. If the HV power supply (PS) has a high resistance off behaviour, the last(s) module(s) in the chain may result forward biased, offering the path to the ground for the currents produced by the other modules. The current flowing through the module ROC circuitry may break it. If the HV power supply off state behaves as a low resistance, the currents produced flow there and there are no forward biased modules. Possible solutions under investigation include: a diode in parallel to the HV regulator and a crowbar circuitry ensuring low impedance to ground when HV is off.

4. Conclusions

The tracker upgrade for the HL-LHC will pose requirements for detector design, electronics and power, which demand innovative solutions. The CMS Outer Tracker and Inner Tracker are developing different schemes to power their front-end electronics. Tests are being performed with non final detector components and cable prototypes.

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