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RD53A chip susceptibility to electromagnetic conducted noise

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The RD53A read-out chip (65 nm CMOS) is a large-scale demonstrator for ATLAS and CMS phase 2 pixel upgrades. It is one of the key elements of the serial powering scheme for the next generation of pixel detectors. The susceptibility of the RD53A chip with respect to external EM noise has an impact on the integration strategies (grounding and shielding schemes) and operating conditions of future Pixel detectors. This paper presents a detailed analysis of the RD53A chip susceptibility to RF conducted disturbances in order to understand and address noise issues of RD53A Chip before the pixel upgrade installation.

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1. Introduction

The extreme high rate operation of the read-out chip at the HL-LHC requires the use of 65nm high density low power CMOS technology with low working voltage (1.2V), resulting in a pixel chip that must be supplied with significant current levels (~2A per chip). During the last years, extensive studies have shown that a serial power distribution system is the only feasible scheme to supply the pixel detector with the required power within an acceptable material budget and power cable losses. Locally, two Shunt–LDO (Low Drop Output) regulators [1] integrated on the pixel chip are needed to allow serial powering connection.

From the point of view of electromagnetic interference (EMI), previous studies have been done on a high energy physics detector [2], but there are not so many precedents [3][4] using this type of powering scheme. In a serial powering scheme, each power group has several modules connected in series and fed with constant current. From the Grounding/EMC point of view this topology is characterized by having only one module connected to the system ground, and the rest floating at different potential levels. To avoid problems on final detector, it is important to measure the noise sensitivity of RD53A chip [5][6] against EM conducted noise, in order to identify critical elements contribution and noise level limits requirements for the power supplies.

2. Noise sensitivity tests and set-up

The main goal of these tests is to define the immunity of phase 2 pixel electronics to RF conducted disturbances:

- Identify and optimize critical elements in prototypes that could reduce the detector performance (Grounding, routing, filtering and decoupling).
- Noise level limits requirements for the power supply units.

These first results will be used as a baseline reference to quantify the impact of different integration options on pixel detector phase II.

To perform these tests, noise currents at different frequencies are injected using bulk current injection probes (BCI) through the power lines of the RD53A chip (both low and high voltage), and then the equivalent noise charge (ENC) per channel is measured. The ENC is obtained by means of a Threshold Scan using the readout software. The measured noise in electrons (ENC_{meas}), and the perturbing injected current is used to compute the transfer function (TF) of RD53A chip against EM conducted noise:

$$TF = \frac{\sqrt{ENC_{meas}^2 - ENC_{ref}^2}}{I_{injected}(mA)} = \boxed{\frac{e_{noise}}{mA}}$$

The reference thermal noise (ENC_{ref}) is the base measurement without any external noise injection.

Figure 1 shows a test set-up picture and a simplified scheme. In this set-up, a Line Impedance Stabilization Network (LISN) is used to avoid the injected noise current going to the power supply, and to close a good coupling path for the common mode current to the ground plane. After that, noise is injected and measured with current probes to the RD53A power lines, and its effect is measured with the ENC parameter obtained using the DAQ system.

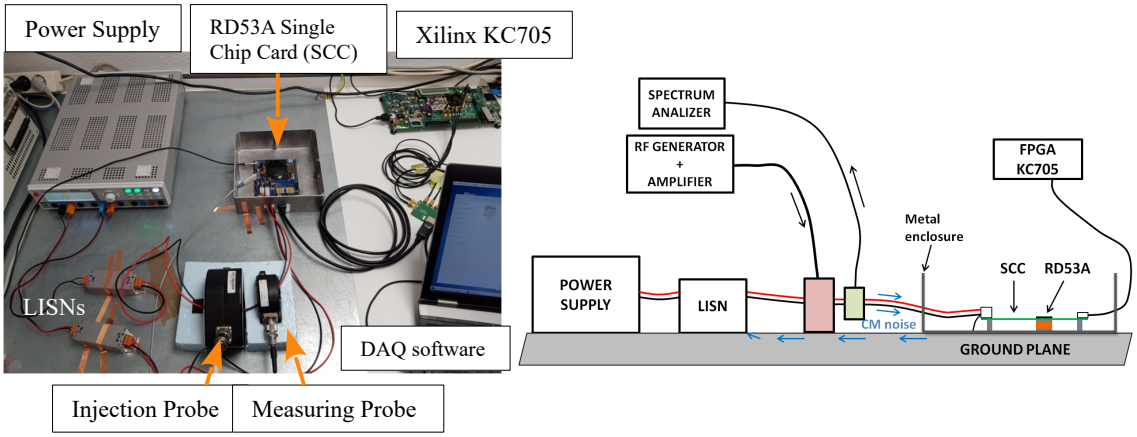

Figure 1: Test set-up picture and scheme.

3. Test results

Several options have been tested in order to understand the contribution to noise sensitivity of the different components and configuration possibilities of this read-out chip:

- RD53A analog FE flavour: Linear, Synchronous and Differential
- Sensor contribution
- Powering conditions: LDO or SLDO mode (Voltage or current power supply)
- Analogue or digital domain sensitivity

3.1 Front-End flavour comparison

Common mode (CM) noise is injected through the analogue power supply line (LDO mode), and the sensitivity of each Front End is compared.

As seen in figure 2 plot, differential FE is the most robust to noise in all range of frequencies.

Synchronous FE is not affected by low frequency noise (<1MHz), due to the fact it is AC coupled. Besides, it shows the typical response of a sampled signal.

Linear FE is the most sensitive to low frequencies but better than Synchronous in the high range.

To simplify tests, the rest of the measurements were performed using only the linear FE. As FE sensitivity differences have been already settled, only one of them is needed to be used as baseline reference.

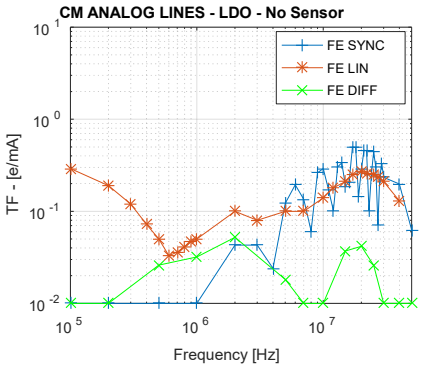

Figure 2: FE flavour comparison

3.2 Sensor Contribution

Noise susceptibility of two different SCC is compared using the linear FE. One SCC with just the bare chip and the other with a chip + sensor.

Figure 3 shows that differences are very small. The presence of the sensor contributes increasing slightly RD53A noise sensitivity.

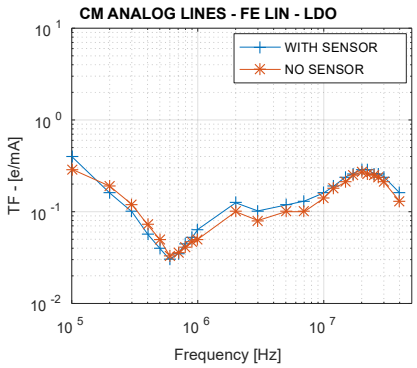

Figure 3: Sensor contribution

This small effect may be caused by the sensor itself generating new noise coupling paths, or just because of different FE configuration.

3.3 Analog and digital power domain sensitivity

RD53A has been designed with two completely separated power domains, one for the analog and one for the digital electronics. Due to set-up limitations, only analog domain could be tested separately, so the comparison is done between analog lines and both digital-analog lines injection.
The results (figure 4) show that the contribution of analog domain to noise sensitivity is dominant in almost all the frequency spectrum. The fact the analog lines are more sensitive to conducted noise was expected.

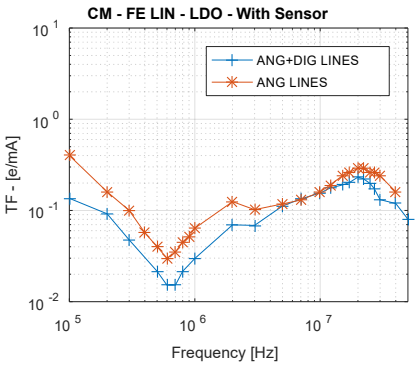

Figure 4: Power domain sensitivity

3.4 Shunt-LDO regulator contribution

Two configurable on-chip shunt-LDO regulators feed separately analog and digital domains. Two different modes, LDO or Shunt-LDO (SLDO), can be selected depending on how the chip is going to be powered: with voltage or current (serial powering). The noise susceptibility of linear FE is measured for these two powering options. Results are shown in figure 5 (left).
The noise sensitivities are quite different, mainly at low frequencies (<2MHz). This high speed linear regulator (BW > 1MHz) has different control loops per mode, which may explain the different frequency response.

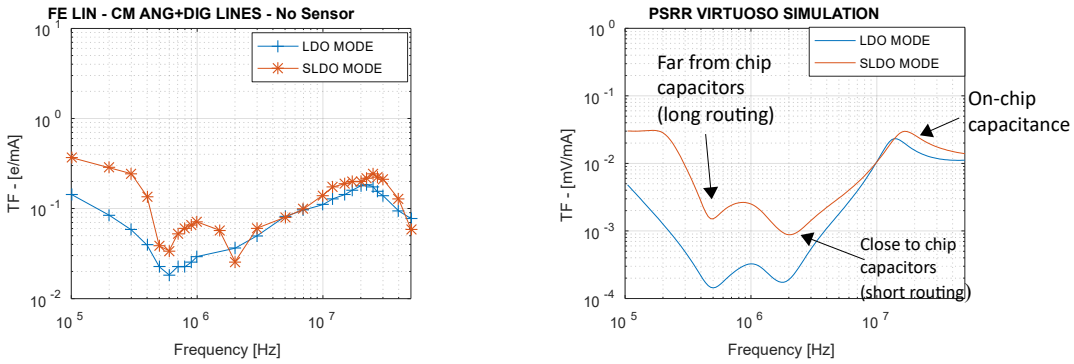

Figure 5: Power mode comparison (left) and regulator PSRR simulation (right)

Preliminary simulations of the Shunt-LDO regulator in Cadence Virtuoso show that its Power Supply Rejection Ratio (PSRR) has a very similar shape compared to noise sensitivity TF.
These simulations are really useful to identify the link of the decoupling capacitors, parasitic elements and regulator response, with noise sensitivity measurements, in order to improve the chip performance even during the design stage. Further simulation model studies are ongoing.

3.5 Comparison with FEI4 chip

As a reference, the RD53A TF is compared with the one of the older FEI4 pixel read-out chip. This is a case of CM noise injection only in analogue power line.
The results show that RD53A is clearly less sensitive to injected noise than FEI4. See figure 6.
It has to be mentioned that FEI4 was tested with direct powering (no internal regulator was used) which could explain the big differences, due to the lower PSRR. Further studies will be done about this point.

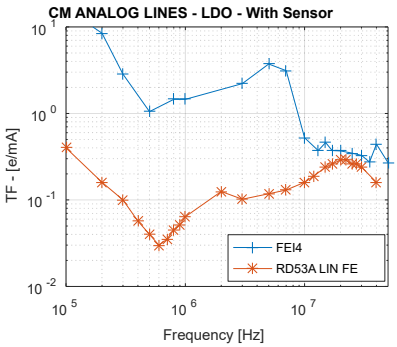

Figure 6: RD53A vs FEI4 comparison

4. Conclusions

These are the first noise studies of RD53A and also of any chip that is intended for serial powering, but still they give useful information. It is also important to comment that the results have been consistent and repeatable, which means the methodology is valid.
Sensor increases the overall noise sensitivity, but just a little. The response against noise of each FE is very different, being the differential FE clearly the most robust. The analog power line is more susceptible than the digital one as expected. SLDO mode is more sensitive than LDO for single chip prototype, confirming that the Shunt-LDO regulator makes big impact on noise sensitivity, and can be confirmed by PSRR simulations of the regulator. There is still work to be done regarding the simulation model, but first results seem promising for predicting the effect of components and layout variations.
The results show that a single chip card RD53A seems to be quite robust to EM and it is a good baseline reference. This reference will allow understanding the contribution of further integration elements such as grounding, filtering, decoupling capacitors or even cooling structures, that will be included on future realistic prototypes and final detectors.
Tests of the HV lines and studies with serial chains of chips are ongoing, and testing of realistic RD53A HDI (High Density Interconnect) modules is planned for the coming months.

References

[1] M. Karagounis et al., *An integrated Shunt-LDO regulator for serial powered systems*, Proceedings of ESSCIRC 2009, Athens, Greece, pg. 276-279 (2009)

[2] M. Iglesias et Al, EMC studies for the vertex detector of the Belle II experiment, Journal of Instrumentation, nº 11, 2016

[3] F. Arteche, C. Rivetta and J. Gómez-Aleixandre, EMC Planning for High-Energy Physics Experiments, IEEE Transactions on Electromagnetic Compatibility, nº 58, 2016.

[4] F.Arteche; C.Esteban; M. Iglesias; C. Rivetta; F.J. Arcega; I. Vila, DC-DC switching converter based power distribution vs Serial power distribution: EMC strategies for SLHC tracker up-grade, Proceedings of 14th Topical Workshop on Electronics for Particle Physics 2009

[5] RD53 web site, http://rd53.web.cern.ch/rd53/

[6] RD53 Collaboration, *The RD53A Integrated Circuit*, CERN-RD53-PUB-17-001 (2017)

[7] S. Orfanelli et al, *Serial Powering Optimization for CMS and ATLAS Pixel Detectors within RD53 Collaboration for HL-LHC: System Level Simulations and Testing*, Proceedings TWEPP 2017-055