PROCEEDINGS OF SCIENCE

TCLink: A Timing Compensated High-Speed Optical Link for the HL-LHC Experiments

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The High-Luminosity Large Hadron Collider (HL-LHC) will pose unprecedented requirements in terms of timing distribution. The overall stability has to reach picosecond-levels between tens of thousands of end-points. To mitigate long-term environmental variations in the high-speed optical links, phase monitoring and online/offline compensation might be necessary. The Timing Compensated Link (TCLink) is a protocol-agnostic FPGA core designed for Xilinx devices that provides monitoring and picosecond-level phase adjustment capabilities with no need for external components. The features can be customized for different user application requirements. A proof-of-concept of TCLink on a setup composed by a Xilinx FPGA evaluation board, the Versatile Link+ [1] and the lpGBT [2] prototype chip will be demonstrated.

Topical Workshop on Electronics for Particle Physics TWEPP2019
2-6 September 2019
Santiago de Compostela - Spain

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PoS(TWEPP2019)057

1. Timing Distribution for High-Luminosity LHC

In order to cope with the high-levels of pile-up expected in the High-Luminosity Large Hadron Collider (HL-LHC), the CMS and ATLAS experiments will use timing information to distinguish between different collisions in the same bunch crossing. This poses challenging requirements in the timing distribution network not to jeopardize the performance of the high-resolution timing detectors which will be installed in the experiments. The stability of the timing distribution network therefore has to reach picosecond-levels. The baseline timing distribution in the HL-LHC experiments consists of thousands of high-speed optical links responsible for delivering the Timing, Trigger and Control (TTC) information as shown in figure 1. The back-end part (where no radiation is present) of the timing distribution network is comprised of FPGAs having multiple transceivers coping with Gbps data-rates. Their front-end counterpart is the radiation-hard low-power Gigabit Transceiver (lpGBT) ASIC [2], a key player to deliver the TTC signals to the front-end chips. Alternative schemes for timing distribution consist of a pure clock being transmitted over the fibre.

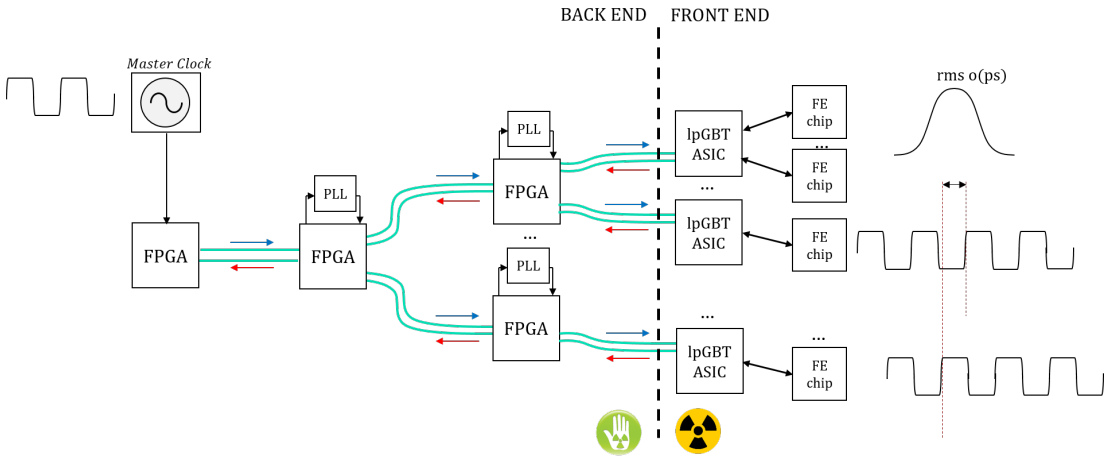


Figure 1: Baseline Trigger, Timing and Control distribution scheme for HL-LHC

In 2018, CERN launched the High-Precision Timing Distribution (HPTD) interest group [3] to study the short- and long-term timing stability performance of different timing components present in the baseline scheme to ensure they can cope with the stringent timing requirements posed by HL-HLC. Studies on the short-term stability of a Versatile Link+ [1] and lpGBT based high-speed optical link have shown that a sub 5-picosecond rms level can be reached [4]. However, long-term stability performance was not yet discussed at that time. Long-term stability due to environmental variations such as temperature might play a key-role in the overall timing distribution stability. The monitoring and online/offline compensation of the phase of the high-speed optical links phase stability might be necessary in order to reach the picosecond-level requirements. As part of the HPTD project, the Timing Compensated Link (TCLink) concept was developed. The TCLink is a protocol-agnostic FPGA core envisaged to mitigate long-term variations in high-speed optical links. The concept is to have monitoring and picosecond-level online adjustment capabilities which can be tailored by the user to best fit his/her own convenience and application requirements. In this paper, a proof-of-concept of the TCLink based on a Xilinx Ultrascale+ FPGA evaluation board, the Versatile Link+ and the lpGBT test chip is demonstrated.

2. Timing Compensated Link

We refer to a timing compensated link when the phase of the recovered clock is stabilized in a controlled-fashion to minimize variations arising from environmental changes in the experiments. Many timing compensated links were developped in the context of physics experiments [5] [6]. The underlying concept is based on three main requirements which can be observed in figure 2:

- A synchronous bidirectional link is established. The slave re-uses its recovered clock for the uplink transmission.
- A high-accuracy roundtrip phase measurement capability is available on the master side. For the compensation, a phase shifter is also required.
- An underlying hypothesis relating the downlink phase variations to the total roundtrip phase variations must be made ($\Delta D = \alpha \times \Delta RT$).

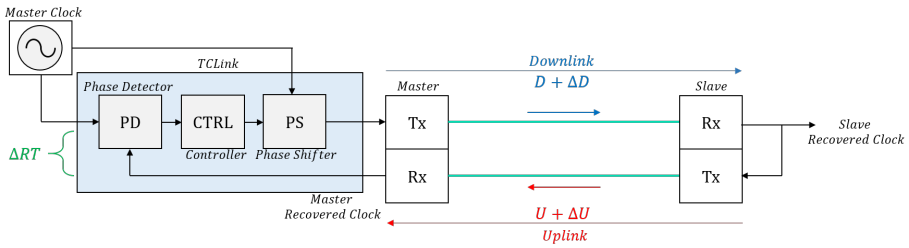


Figure 2: TCLink Principle

For this proof-of-concept, a timing compensated link fully integrated in the FPGA was developed. The phase measurement is performed using a technique called Digital Dual Mixer Time Difference, discussed in [6]. The phase shifter is the Xilinx Ultrascale transmitter phase interpolator [7] controlled by the HPTD IP Core [8].

The controller block is implemented using techniques from the All-Digital PLL field [9] [10]. The controller is shown in more detail in figure 3. The loop-control is used to set particular dynamics for the system. A sigma-delta modulator is used to control the phase shifter, issuing a stream of pulses with the information of either advance or retard phase. For this first proof-of-concept, we assume a symmetry hypothesis ($\Delta D = 0.5 \times \Delta RT$). In future implementations, the user will have the flexibility of choosing its own α coefficient.

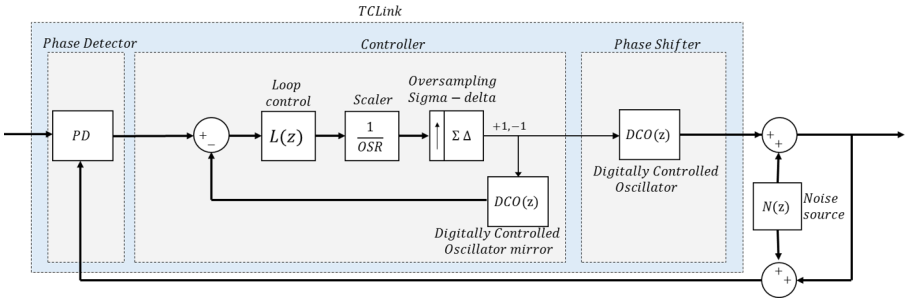


Figure 3: TCLink Control Scheme

3. Experimental Results

The setup used for the first TCLink tests is shown in figure 4. This implementation uses the Versatile Link+ [1] as an example to demonstrate the TCLink functionality. Temperature variations in the optical fibers are emulated using a climatic chamber and the phase between the reference clock [11] given to the FPGA evaluation board [12] and the recovered clock of the lpGBT [2] is measured with a scope. The data transmitted in the downlink (2.56Gbps) and uplink (10.24Gbps) directions are a PRBS-7 pattern encoded with the lpGBT encoding scheme.

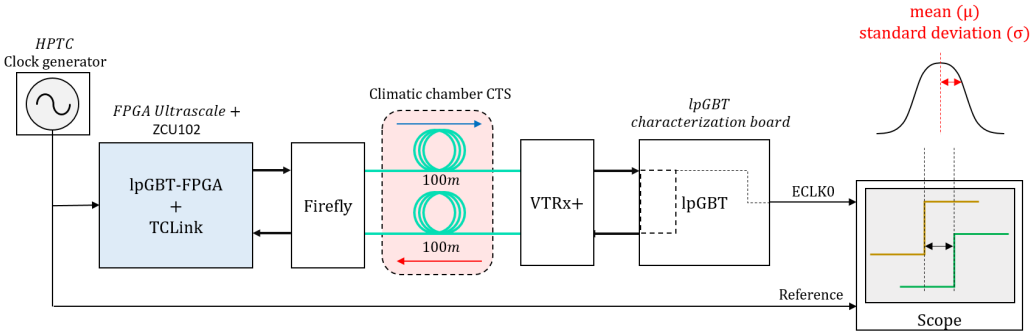
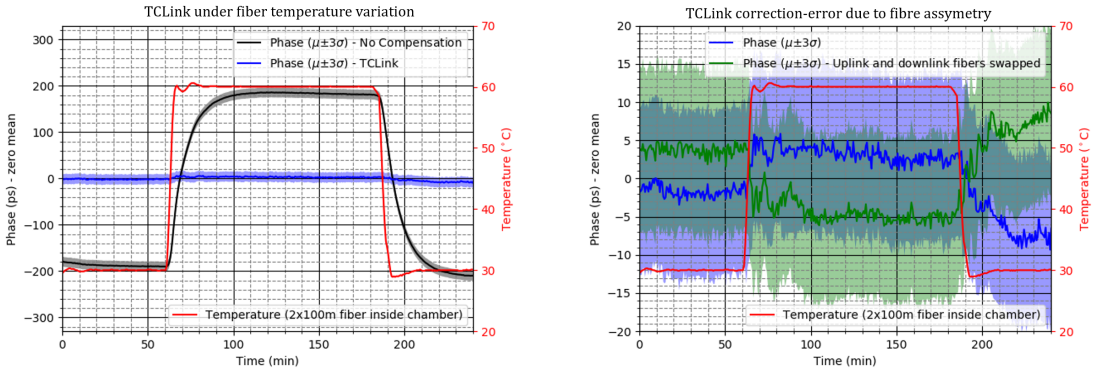


Figure 4: Fiber temperature test setup

It can be observed in figure 5a that TCLink successfuly compensates for phase variations arising from the optical fibers. It can also be noted in figure 5b that the remaining error (around 5ps) is due to the asymmetry between the downlink and uplink fibers.



(a) TCLink vs. uncompensated link

(b) TCLink error due to fibre asymmetry

Figure 5: Fiber temperature test results

A small penalty in terms of phase-noise can be observed in figure 6 ($150fs$ integrated phase-noise). The loop compensation bandwidth is around 100Hz for this design. This negligible penalty can be potentially made even smaller by changing the controller loop parameters.

4. Conclusions and Next Steps

In this paper, a timing compensated link fully integrated in the FPGA was demonstrated. It can

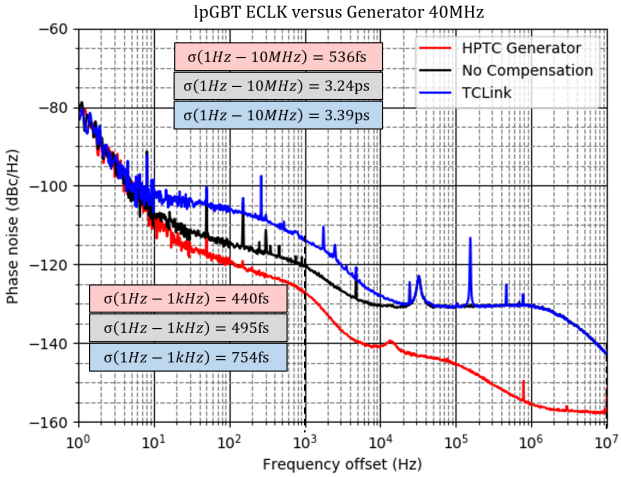


Figure 6: Phase-noise of chain implementation

provide an independent compensation for multiple links in a single Xilinx-based FPGA. Additional tests will be performed to analyze the impact of FPGA usage and temperature on the TCLink performance. A full characterization campaign under realistic experimental conditions is foreseen.

We plan to provide the interested users with an example design and an application note on how to use the TCLink core.

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