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VMM3a: an ASIC for Tracking Detectors

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The VMM3a is a custom Application-Specific Integrated Circuit. It will be used as the front-end chip for both Micromegas and sTGC detectors of the ATLAS Muon New Small Wheel upgrade at CERN. Due to its flexibility and several configurable parameters, it has also been proposed for a variety of tracking detectors in other experiments. The VMM integrates 64 independent channels, each providing amplitude and timing measurements in digital or analog format. The chip has undergone three major revisions and a minor one, with the first prototype being produced in 2012. It began as a purely analog chip, providing timing and amplitude measurements for digitization by external analog-to-digital converters, while its latest version combines analog circuitry, embedded digitizers, buffers, radiation-protection logic and modules that produce fast signals for triggering, all in one chip - the VMM3a. In this document, the design aspects of the VMM3a as a production front-end chip will be presented.

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1. Introduction

The upgrades of the Large Hadron Collider (LHC) at CERN in 2019-20 (LS2) and 2024-26 (LS3) will increase the instantaneous luminosity. To cope with the increased particle flux, the LHC experiments will be upgraded as well. During LS2, each of the so-called "Small Wheels" of the ATLAS muon spectrometer are planned to be replaced by the "New Small Wheel" (NSW), which will be comprised of two gaseous detector technologies, namely the Micromegas (MM), mainly used for track reconstruction, and the small strip Thin Gap Chambers (sTGC), mainly used for triggering [1]. Both detector types will provide trigger and tracking information, resulting in a fully redundant system. The 2.4 million readout channels of those chambers will require a new generation of electronics to read them out. The electronics must be able to endure a harsh radiation environment, while at the same time be compatible with the upgraded trigger rates, which are expected to reach a frequency of 1 MHz and 400 kHz in the two-stage trigger scheme of ATLAS. The cornerstone of the NSW's electronics system is the VMM Application-Specific Integrated Circuit (ASIC), which will connect to the detector readout elements to provide trigger and tracking data to ATLAS [1, 2]. The overall connectivity of the VMM with other front-end electronic devices of the NSW are presented in Figure 1.

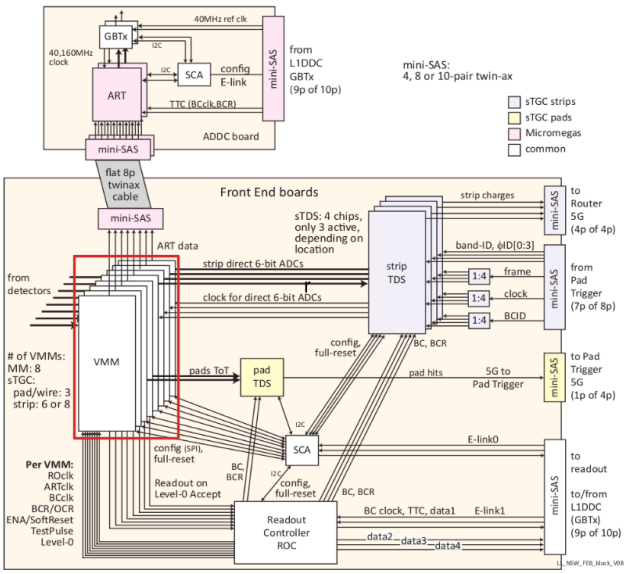

Figure 1: Overview of the VMM's connectivity with other ASICs of both detector technologies within the NSW electronics scheme. It is being configured by the Slow Control Adapter (SCA). It sends tracking data to the back-end readout system via the Read-Out Controller (ROC) and it forwards MM and sTGC trigger data to the back-end trigger processing system via the Address-in-Real Time (ART) ASIC and the Trigger Data Serializer (TDS) ASICs respectively.

2. Overview and Readout Paths

The VMM has been developed at Brookhaven National Laboratory and fabricated in the 130 nm Global Foundries 8RF-DM process (former IBM 8RF-DM). It can be used in a variety of charge-interpolated tracking detectors, packaged in a Ball Grid Array with outline dimensions of 21 ×

21 mm^2. The chip is composed of 64 discrete channels. Each channel connects to a detector readout element and performs charge amplification, discrimination and precise pulse amplitude and timing measurements through Analog-to-Digital Converters (ADCs). An architectural overview of each channel can be seen in Figure 2. Radiation-wise, it is expected that the VMM will be exposed to a total ionization dose of 100 krad, but its Triple Modular Redundancy (TMR) architecture allows for it to operate smoothly, even after that dose. The chip has a plethora of configuration parameters that the users can tune according to their needs. This is done via the SPI protocol, which makes it possible to shift 1728 bits into the ASIC's configuration registers.

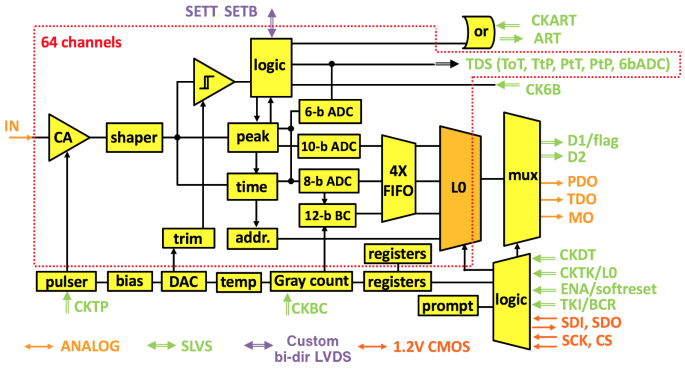

Figure 2: Block diagram of the VMM ASIC. The charge amplifier on the left-hand side collects and integrates the charge that goes through a shaper [4]. A configurable threshold circuitry activates the rest of the channel's functionalities. These can be divided into two groups, one used for the trigger path and another for the readout path. The latter mainly involves digitizing the signal's amplitude and timing information using a 10-bit and an 8-bit ADC respectively, before buffering the data into dedicated memories. The trigger primitives provided by the VMM are created either by digitizing the pulse's amplitude using a rapid 6-bit ADC, by asserting a single-bit Time-over-Threshold (ToT) signal, or by forwarding the 6-bit address (ART) of the chip's channel that registered an event first [2].

The VMM's input MOSFET is a p-channel with gate area of $L \times W = 180\,\text{nm} \times 10\,\text{mm}$ (200 fingers, 50 µm each) biased at a drain current $ID = 2\,\text{mA}$; this corresponds to an inversion coefficient $IC \approx 0.22$, a transconductance $g_m \approx 50\,\text{mS}$, and a gate capacitance $C_g \approx 11\,\text{pF}$. The transistor-level schematic of the charge amplifier can be found in [3]. The filter (shaper) is third-order (one real pole and two complex conjugate poles) designed in delayed dissipative feedback (DDF), with adjustable peaking time (25, 50, 100, and 200 ns) and stabilized, band-gap referenced, baseline. The DDF architecture offers higher analog dynamic range with a relatively high resolution with respect to more classical configurations, due to its architecture, which roughly involves delaying the resistive feedbacks from the furthest available nodes along the shaping chain [4]. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC) [2]. The chip's front-end amplifier has adjustable gain and integration time, and can handle signals of opposite polarities and a high range of capacitances, while being low on power consumption. Finally, given the requirements of the NSW, the noise requirements are deemed to be within specifications (see Figure 3).

2.1 The Readout Path

Once a channel accumulates charge which creates a pulse that crosses the user-defined threshold, the channel processes and digitizes the pulse's properties in 250 ns (essentially the channel's dead-

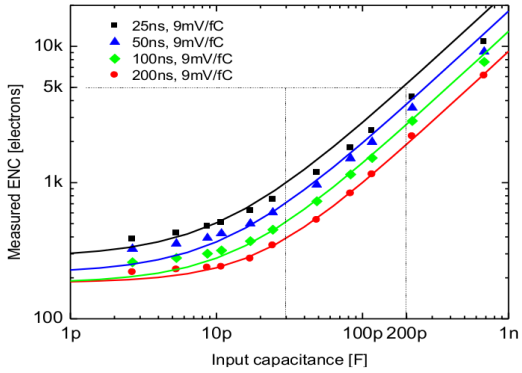

Figure 3: The VMM input channel noise as a function of all four peaking times at a gain of 9 mV/fC [2]. The solid lines represent the simulation results, while the markers are extracted from experimental data.

time) before buffering the data. The peak detector measures the pulse's amplitude and stores the current-based measurement into an analog memory. The 10-bit ADC that digitizes this current is based on an innovative flash converter architecture that involves driving the current to a series of cells that perform successive summation of reference currents and comparisons to the current-under-measure [5]. The result is a 10-bit word, called PDO (Peak-Detector Output), that provides a $\sim$ 0.4 fC charge resolution, depending on the gain [2]. The timing measurement is performed via a Time-to-Analog-Converter (TAC), which involves a circuit that starts charging at a constant rate either upon the detection of a peak, or at the crossing of a threshold. The ramping duration is adjustable (60, 100, 350, and 650 ns). The ramp is halted at the next falling-edge of the reference clock, which for the ATLAS implementation is the Bunch-Crossing (BC) clock with a frequency of 40.079 MHz. The resulting current is stored and then digitized by an 8-bit ADC. The 8-bit word is called TDO (Time-Detector Output), and provides a timing resolution of $<$ 1 ns, depending on the TAC's ramp duration and the peaking time [2]. The two ADC values, alongside the BCID (a coarse timing timestamp by a 12-bit Gray counter that increments at each rising-edge of the reference clock) and the channel ID, are stored into a FIFO, before being forwarded to the L0 selection circuitry. This logic allows for the VMM to select muon-related data upon reception of a trigger signal and forward them to an external device (for the ATLAS implementation, this is the ROC - see Figure 1). The readout device issues a trigger that gets timestamped by the VMM, which then applies a configurable offset to this timestamp and compares it to the stored event in the BCID FIFO. Channel hits that are matched within a window are forwarded towards the readout device via two data lines with 8b/10b encoding, resulting in an effective bandwidth of 512 Mbps.

2.2 The Trigger Path

The VMM also operates at a faster mode, used for triggering. For the MM trigger scheme, the ART mode is used. Upon the detection of a pulse peak, or upon a signal crossing of a user-defined threshold, the chip outputs the channel address that this peak is detected on. Depending on the chosen configuration parameters on the VMM, the total latency of the streamed ART address can be within $\sim$ 15 ns, or $\sim$ 20 ns plus the peaking time. This latency is the sum of several delays, some of which are the 5 ns delay between the peak and the peak-found signal, the 5 ns digital latency

from the comparator firing to the leading edge of the ART and the 5 ns digital latency from the peak-found signal to the leading edge of the ART. The 6-bit channel address plus a flag are sent to an external device that aggregates trigger primitives at a rate of 320 Mbps. For the sTGC detector technology, the VMM provides trigger information via its 64 direct timing outputs, one for each of its channels. Each channel implements a fast digitization 6-bit ADC, that provides a coarse, but rapid (the conversion takes up about 40 ns, including the channel reset), amplitude measurement of the pulse. The conversion starts immediately at the peak time and the data are streamed at each output. Another way to operate the direct timing outputs is in the Time-over-Threshold (ToT) mode. As long as a pulse is above the threshold, the VMM outputs a digital ToT pulse, in one of its direct-timing output pins with a latency of about 14 ns.

3. Conclusions

The VMM has been designed to serve the readout needs of the NSW upgrade of the ATLAS detector. It will provide tracking and triggering information to ATLAS, while being able to cope with the high trigger rates and the harsh radiation environment of the NSW. At the time of writing of the present document, about 34000 chips of the production version of the ASIC, the VMM3a, have been tested with a yield of 73% across 113 wafers[1]. A tracking and triggering all-in-one chip, the VMM can make precise measurements on the detected charge with an accuracy of ~ 0.4 fC and the pulse's timing with a resolution of < 1 ns, depending on the mode of operation. Its amplifier can operate with both signal polarities and a variety of gains. The chip can integrate charge from 25 up to 200 ns and besides the precise measurements that were mentioned above, it can also produce trigger primitives at a very low latency and minimal dead time. These characteristics deem it flexible enough to be applicable to a variety of other potential experiments and detector technologies.

Acknowledgments

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[1] With room for improvement given potential changes in the fabrication process.