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FAST: a 30 ps time resolution front-end ASIC for a 4D tracking system based on Ultra-Fast Silicon Detectors

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Abstract

The UFSD group of Turin is working on developing custom front-end electronics for the read-out of thin silicon sensors with moderate internal gain, the so called Ultra-Fast Silicon Detectors-UFSD, aiming at applications that require very precise time tagging. The activity of the group is mainly focused on meeting the requirements of the next generation of High Energy Physics (HEP) colliders where time tagging is a fundamental tool that can be exploited to distinguish events overlapping in space but separated in time by a few tens of pico-seconds.

FAST, a 20 channels low power ASIC is presented in this paper. This prototype has been designed to reach a 30 ps time resolution when coupled to UFSD. To investigate the best ASIC architecture, three different design solutions of FAST has been developed with variations regarding the amplification stages and component-level technical choices.

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1. Introduction

The activities of the Turin UFSD group [1] are centered on the design and characterization of silicon sensors and on the development of front-end electronics. While the main interest is HEP, the UFSD group participates also in applied physics activities e.g. R&D for particle therapy. In both fields, having fast sensors with high spatial and time resolution is currently crucial to achieve performances beyond the present for state-of-the-art projects. The next generation of HEP colliders will push higher the luminosity frontier and a direct consequence is that experiments worldwide will focus their effort on the development of tracking systems, silicon sensors and front-end electronics, with very strict requirements in terms of timing capabilities. This is the case of the High-Luminosity upgrade of the LHC (HL-LHC), where the new design foresees a pile-up factor of 150-200 events per bunch crossing. To mitigate the consequences of high pile-up, both ATLAS, with the High Granularity Timing Detector (HGTD), and CMS, with the MIP Timing Detectors (MTD), are pursuing time tagging projects with a $\sim$30 ps time resolution.

The measurement of the Time of Arrival of a particle is affected by uncertainties coming both from the sensor used to detect particles and from the readout electronics used to measure the weak signals generated by the particles hitting the sensor. To improve the time resolution, signals with high amplitudes and short rising time are key points. This requirement leads to the optimization of both silicon sensor and readout electronics. In this context, Ultra Fast Silicon Detectors (UFSD) [2] are proposed as a good example of optimized sensors for time measurements, due to their capability to generate signals short in time and large in amplitude. For what concerns the contribution of the readout electronics, the slew rate and the front-end noise are the main characteristics influencing the timing performances.

In this paper, we present FAST, a low power front-end ASIC developed for high precision timing measurements with UFSD sensors. This prototype is the results of a microelectronics development plan started in 2016, evolved firstly with TOFFEE [3], a prototype ASIC meant for timing applications and successively with ABACUS [4], a ion counter developed for medical physics applications with UFSD. A short description of UFSD is given in Section 2 whereas the description and the simulation results of the FAST ASIC is provided in Section 3 and 4, respectively.

2. Ultra Fast Silicon Detectors

Ultra Fast Silicon Detectors are thin silicon Low Gain Avalanche Diodes (LGAD) with internal gain able to produce large signals as required to measure time accurately. The internal gain is based on charge multiplication generated by carriers drifting in an electrical field of about $\sim$300 kV/cm [2]. Under these conditions, the carriers acquire the kinetic energy necessary for the production of new electron-hole pairs. Several parameters such as thickness, resistivity and area have been optimized in UFSD to get the best time resolution. These sensors tolerate a radiation up to 10^{15} n_{eq}/cm^2 [5]. The properties of UFSD as timing detectors have been extensively tested with laser sources and particle beams. Several results are reported in [6].

3. FAST as readout electronics

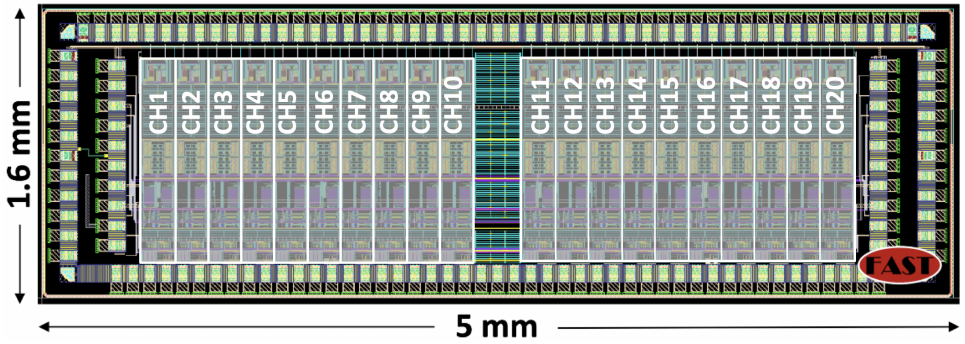


Figure 1: Layout top view of the 1.6 mm $\times$ 5 mm FAST prototype.

FAST (Front-end Amplfiers for Silicon detectors in Timing applications) is a prototype developed combining the know-how coming from the design and characterization of two ASICs dedicated to the readout of UFSD: ABACUS [4] (Asynchronous logic Based Analog Counter for Ultra fast silicon Strips) and TOFFEE [3] (Time Of Flight Front End readout Electronics). The former is a single ion counter front-end ASIC developed in 2018 for particle therapy applications in the framework of the INFN MoVe-IT (Modeling and Verification for Ion beam Treatment planning) project [7]. The latter has been developed in 2016 to fulfill the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) time resolution requirements of 30 ps [8, 9]. Both prototypes have been designed in a 110 nm commercial technology node and dedicated characterization campaigns showed milestones-matching results.

FAST has been developed to cope with the requirements of high time resolution but paying particular attention to reduce the power consumption by a factor 10 compared with the previous ASICs. Furthermore, the signals shaping introduced by the FAST front-end allows managing input

Channels number	20
FAST flavors	3
Operation voltage	1.2 V
Die size	1.6 x 5 mm^2
Sensor capacitance	2-6 pF
SNR	60
RMS noise	1 mV
Front-end power consumption	$<$ 2 mW/ch
Driver power consumption	1 mW/ch
Time walk correction	based on ToT
MPV	8 fC
Input dynamic range	1-60 fC

Table 1: FAST post-layout design specifications

signal rates up to few hundreds of MHz. The prototype is designed in a commercial 110 nm CMOS technology and it is specifically optimized for UFSD of 3-6 pF in a range of temperature between -30 and +50 Celsius degrees. The chip provides a 25 ps time resolution and the capability to detect single ions with rates up to 200 MHz with a 6 pF UFSD. FAST is a 1.7 mm $\times$ 5 mm chip (Figure 1) consisting of 20 channels which send the information off-chip in LVDS (Low-Voltage Differential Signaling) format. The most important specifications used for the design are reported in Table 1.

The channel architecture, depicted in Figure 2, consists of a Trans-Impedance Amplifier (TIA), a second amplification stage based on a common source amplifier (CS), a two stages leading edge discriminator (DISC1 and DISC2), a Pulse Width Regulator (PWR) to tune the digital output duration and a LVDS driver.

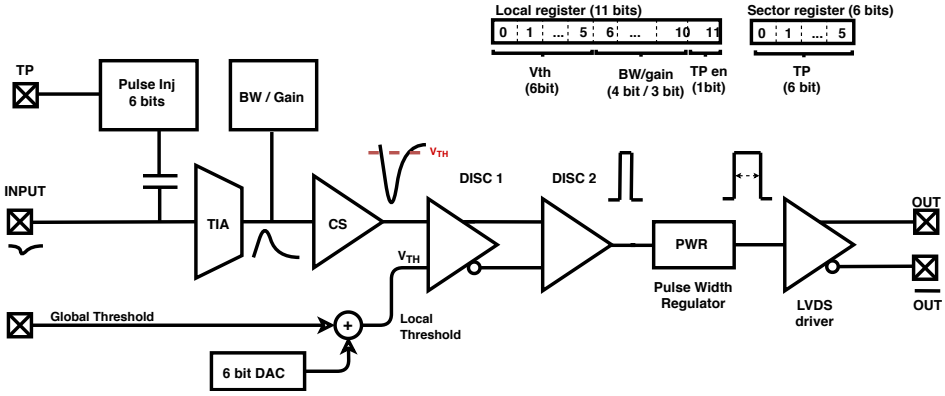
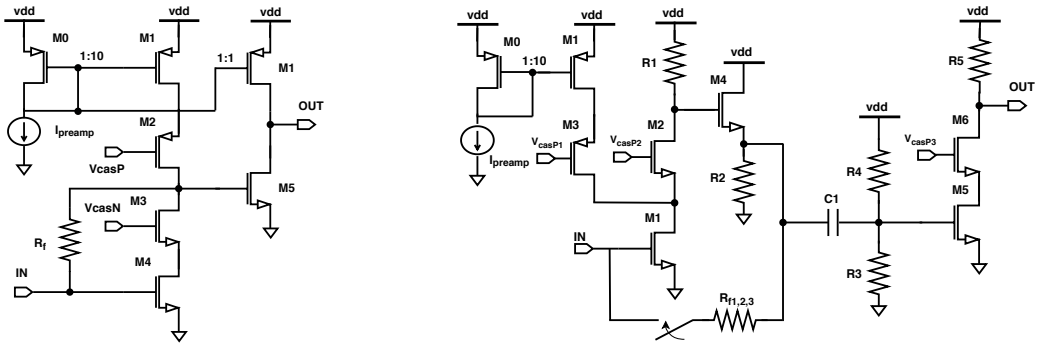


Figure 2: Block diagram representation of a FAST channel.

FAST has been designed in three different flavors which differ in the front-end amplifier. The design aims to optimize the noise-to-slope ratio of the front-end which is fundamental to meet the target time resolution. These flavors are named REG, EVO1 and EVO2. The front-end amplifier used in the REG flavor, shown in Figure 3a, is based on a cascoded common source amplifier close in feedback by a resistor R_f of 20 kΩ. This TIA stage is followed by a CS that provides a second amplification. The bandwidth of the front-end is 70 MHz and it allows increasing the noise-to-slope ratio by keeping the noise low. EVO1 and EVO2 flavors have been designed with the front-end architecture shown in Figure 3b. The EVO front-ends consist of a Broad-Band (BB) core amplifier close in feedback by the resistor R_f which can be selected among 3 different values. Thanks to the usage of passive loads and NMOS cascodes, the bandwidth of the broad-band reaches 400 MHz. Such a bandwidth allows increasing the slope of the output signal and thus also the noise-to-slope ratio. A dedicated branch has been used in the BB amplifier to tune the current of the stage. The first stage is then AC coupled to a CS stage which provides a second amplification. The AC coupling has been used to minimize the impact of the DC variations due to process mismatch affecting the second stage. The power consumption for both amplifiers is around 1.4 mW, rising to 3 mW when including the discriminator stages. The LVDS driver power consumption is 1 mW/ch. A technology study has been included in the project, taping out EVO1 using standard transistors and EVO2 using RF transistors.

Additional features have been introduced around the main blocks of the chain to tune and test the channels performances. Among these, a programmable charge to voltage gain of the TIA



(a) Front-end used for the REG flavor.

(b) Front-end used for the EVO flavor.

Figure 3: FAST Front-end amplifiers. On the left the architecture solution adopted for REG and on the right the EVO one.

amplifier: low gain values allow to increase the ions detection rate capability but degrade the jitter performance while high values improve the time resolution but reduce the maximum rate which can be tolerated before saturate the amplifier. Fine threshold tuning through a 6 bits local DAC and a programmable block for the test pulse injection are implemented at channel level.

4. Simulation results

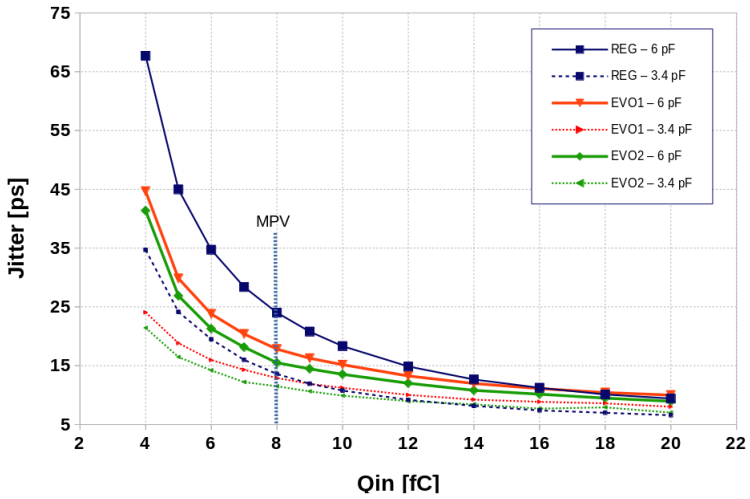


Figure 4: Jitter simulation results as a function of the injected charge Q_{in}. The different curves represent the three FAST prototype flavors, coupled with two values of detector capacitance, 3.4 pF and 6 pF.

Table 1 reports the FAST technical features as resulting from post-layout simulations. Among these numbers, it is worth mentioning a large Signal to Noise Ratio (SNR) of 60 for a MIP, and a power budget in the order of few mW per channel. Concerning the timing performances, Figure 4 shows the FAST jitter as a function of the injected charge, for two different values of detector

capacitance: 3.4 pF and 6 pF. It is possible to notice that, considering a 8 fC injected charge, the Most Probable Value (MPV) generated by typical UFSD with a 55 μm sensor thickness and gain factor of 15, the expected jitter is lower than 30 ps for all the three FAST flavors. This value is very promising and fully satisfies the design goal.

5. Conclusion and Acknowledgments

Accurate simulation of the novel FAST ASIC taking into account UFSD model, generated with Weightfield2 [10], predicts a 35 ps time resolution with 6 pF sensors. This value takes into account the contribution coming from the electronics, the sensor, and time walk. The contribution of the electronics is estimated to be of the order of 25 ps. The promising simulation results have to be compared with on-silicon data. FAST ASICs have been received in late September 2019 and a characterization campaign is planned for 2019-2020.

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References

[1] *http*: /*cern.ch*/*nicolo*

[2] Hartmut F-W Sadrozinski and Abraham Seiden and Nicolò Cartiglia, *4D tracking with ultra-fast silicon detectors*, Reports on Progress in Physics, 2-026101, 2018

[3] F. Cenna et all *TOFFEE: a full custom amplifier-comparator chip for timing applications with silicon detectors*, JINST 12 C03031, 2017

[4] F. Fausti, J. Olave, G. Mazza, V. Monaco, R. Sacchi, R. Cirio *ABACUS : Two fast amplifiers for the readout of LGAD detectors.*, JINST 12 C03031, 2017

[5] Z. Galloway and et al., *Properties of HPK UFSD after neutron irradiation up to 6E15 n/cm2, (2017)*, 1707.04961, 2017

[6] N. Cartiglia et al., *Beam test result of a 16 ps timing system based on ultra-fast silicon detectors*, Nucl Istrum. Meth. A 850 (2017) 83 [arXiv:1608.08681].

[7] http://www.tifpa.infn.it/projects/move-it/

[8] CMS-TOTEM collaboration, *CMS-TOTEM precision proton spectrometer*, CERN-LHCC-2014-021 (2014) [TOTEM-TDR-003] [CMS-TDR-13].

[9] CMS-TOTEM collaboration, *Addendum to the TOTEM TDR: timing measurements in the vertical roman pots of the TOTEM Experiment* LHCC document CERN-LHCC-2014-020 including questions/answers from/to the referees, CERN-LHCC-2014-024 (2014) [TOTEM-TDR-002-ADD-1]

[10] F. Cenna, et al., Weightfield2: a fast simulator for silicon and diamond solid state detector, NIM A 796 (2015)