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Analog front-end characterisation of the RD53A chip

Natalia Emriskova[*†]
CERN, Université de Strasbourg
E-mail: natalia.emriskova@cern.ch

For the Phase-2 upgrade of ATLAS and CMS tracking detectors, a new pixel detector readout chip, with a 50 µm × 50 µm pixel size, is being designed in 65 nm CMOS technology by the RD53 collaboration. A large-scale demonstrator chip called RD53A, is now available. The RD53A chip was designed to withstand a total ionizing dose of 500 Mrad, to operate at thresholds below 1000 e^-, with a noise occupancy below 10^{-6} and to cope with a hit rate up to 3 GHz cm^{-2}. It contains design variations in the pixel matrix, among which are three different analog front-ends. A dedicated program of testing and detailed characterization has been devised and carried out to qualify the three front-ends. The key performance parameters for the operation of a pixel detector at High Luminosity LHC, against which the three circuits have been evaluated, are the amount of spurious hits in the detector, caused by the noise and the late hits and the dead time driven by time-over-threshold calibration.

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[*]Speaker.
[†]On behalf of the CMS Collaboration.

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1. High luminosity upgrade and the RD53A chip

The Phase-2 upgrades of silicon pixel detectors at HL-LHC experiments will cope with extreme operating conditions, such as a fluence reaching 2.3×10^{16} $n_{eq}cm^{-2}$, a total ionizing dose up to 1.2 Grad and a hit rate up to 3 GHzcm^{-2} [1], therefore a new generation of pixel readout chip is being designed in 65 nm CMOS technology by the RD53 collaboration, a joint effort between ATLAS and CMS. A large-scale demonstrator chip of 20.0×11.8 mm^2 (half size of the final chip), called RD53A, was designed with a pixel matrix composed of 400×192 square pixels, with a 50 µm pitch [2]. The readout chip can be bump-bonded either to sensors with square pixels of the same size or to rectangular pixels of 100×25 μm^2, thanks to electrode routing in the sensor [1].

2. Three analog front-ends in one chip

In the RD53A chip, three independently designed analog front-end (AFE) circuits were implemented to allow for comparison of different design options. They are called synchronous (SYNC), linear (LIN) and differential (DIFF) front-end. A detailed description and schematics can be found in [2, 3, 4]. All three front-ends are based on a charge-sensitive amplifier and use the time-over-threshold counting. SYNC and LIN use a Krummenacher circuit for the feedback loop [5], while DIFF uses a simple MOS in the feedback for continuous reset and a low-pass filter for the leakage current compensation. Moreover, DIFF uses a differential gain stage in front of the discriminator and implements a threshold by unbalancing two branches. Both LIN and DIFF front-ends have a time-continuous discriminator, with a per-pixel trimming DAC for threshold equalization, while SYNC has a synchronous discriminator and is using an auto-zeroing technique, consisting in a periodic acquisition of the baseline [3].

The three AFEs were evaluated against CMS requirements, which are: threshold of 1000 e^- (typical charge release by a MIP in a 100 µm thick sensor is about 6000 e^-), noise occupancy below 10^{-6}, 1 % dead time in the innermost layer, given a per pixel hit rate of 75 kHz, and radiation hardness up to at least 600 Mrad. The key measurements that allowed CMS to choose the most suitable AFE are presented in the following sections. All the results were obtained using the calibration injection circuit (same for the three AFEs) [2] and with RD53A chips bump-bonded to sensors with rectangular pixels, operated at cold temperature (about $-10\,^{\circ}C$).

3. Dead time and time-over-threshold calibration

The dead time is a crucial parameter for the operation at high luminosity due to the high pile-up. It can be reduced by increasing the preamplifier discharge current, which makes the preamplifier discharge faster. Simulations show that in order to achieve the required 1 % dead time in the innermost layer, it is necessary to discharge an equivalent input charge of 3000 e^- within one LHC clock cycle (25 ns) [6]. This corresponds to a typical signal of 6000 e^- having a time-over-threshold (TOT) of two clock cycles. The TOT response of the three AFEs, measured using a charge injection of 6000 e^-, for different preamplifier discharge currents is shown in Figure 1. All three AFEs can reach the required TOT response. SYNC and LIN can also discharge faster, while DIFF shows a saturation of the preamplifier discharge current DAC and would be operated at its limit.

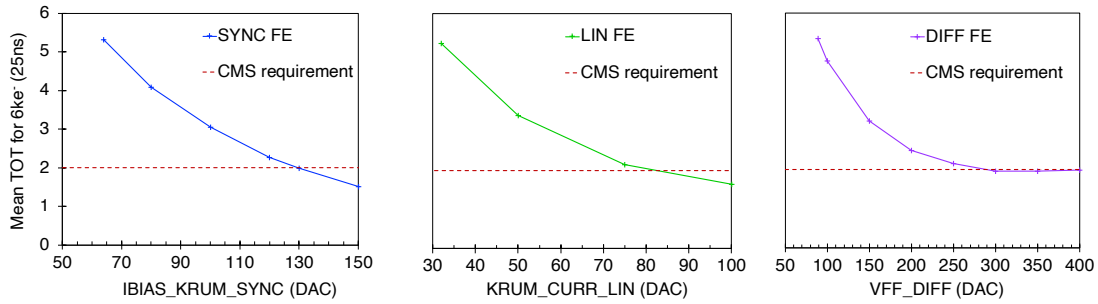

Figure 1: Mean time-over-threshold for an equivalent input charge of 6000 e^- as a function of the DAC settings of the registers driving the discharge current in each AFE.

4. Evaluation of noise levels

Noise performance was qualified by the number of noisy pixels and the equivalent noise charge (ENC). The latter was evaluated by measuring occupancy versus threshold (S-curves). A pixel was declared noisy, and masked, if it fired more than 10 times in 10^7 triggers at the threshold of 1000 e^- for a chip without sensor and 1200 e^- with sensor. The fraction of masked pixels is shown in Figure 2 on the left and the average ENC of the non-masked pixels on the right. As expected, the measurement shows that when a sensor is connected to the chip, the noise is higher due to the sensor load capacitance. However, the noise is significantly larger for SYNC with the number of noisy pixels increasing from 0.04 % to 1.2 %, which is probably due to a smaller phase margin.

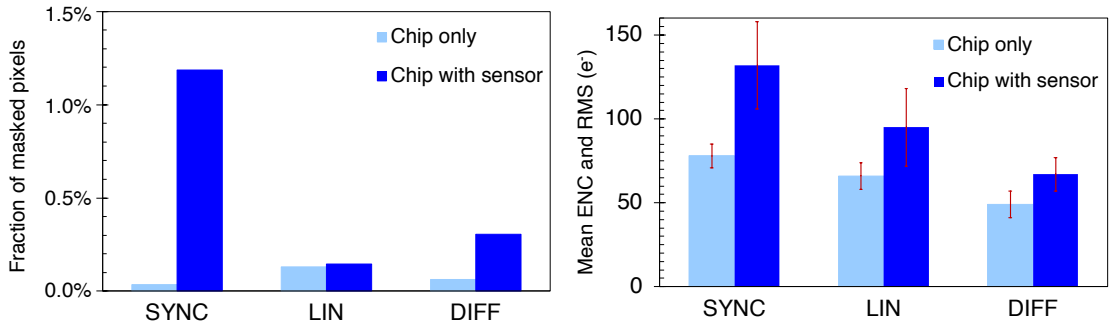

Figure 2: Fraction of masked pixels (left) and the equivalent noise charge after masking (right).

5. Noise occupancy at fast discharge

Increasing the discharge current allows to reduce the dead time, as mentioned before, but it also makes the AFE less stable, because it reduces its phase margin and therefore it is likely to induce more noise. Hence, the noise was also evaluated at a so-called "fast discharge" (mean TOT = 2 clock cycles for 6 ke^-), while the previous noise measurement was obtained at "slow discharge" (mean TOT = 5.3 clock cycles for 6 ke^-). First, every pixel with more than 100 hits in 10^6 triggers was declared noisy and masked. The fraction of masked pixels is shown in Figure 3 on the left and on the right is the noise occupancy after masking, defined as the number of noise hits

per pixel and per trigger, measured over 10^6 events. DIFF shows excellent noise performance, with almost no noisy pixels. The noise occupancy of LIN and DIFF satisfies the requirements, while SYNC appears to be the noisiest of the three with almost 4 % of noisy pixels. The higher noise in this AFE, getting worse with the fast discharge settings, would require further investigation and the SYNC front-end would need a design modification to be suitable for the operation in the innermost layer of the CMS tracker.

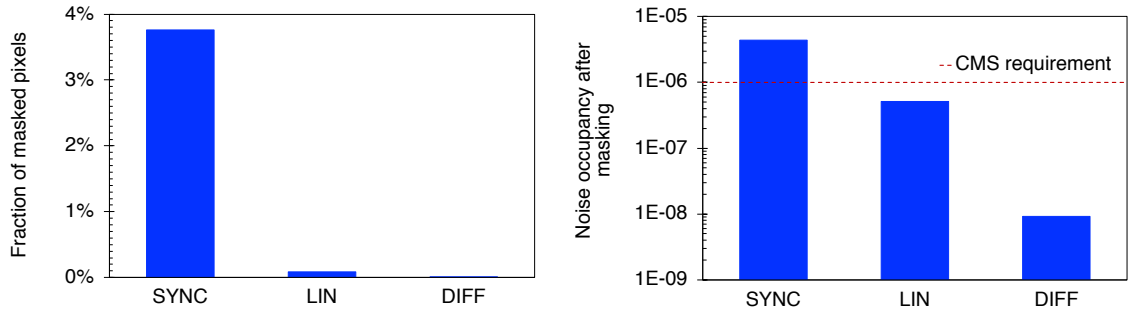

Figure 3: Fraction of masked pixels (left) and the noise occupancy after masking (right) for the innermost layer scenario, i.e. 1000 e^- threshold and fast discharge of the preamplifier.

6. Fraction of late hits

In order to predict the fraction of hits detected late and appearing as spurious hits in the detector, a comparative evaluation was done by combining the measurement of the front-end time response with the hit time-of-arrival and amplitude information from Monte Carlo simulation. The time response was measured by injecting calibration pulses with different timing with respect to the rising clock edge and with different signal amplitudes. Then the probability of a hit to be assigned to a given clock cycle was estimated. An example of such a measurement for LIN is shown in Figure 4 on the left. The edge of the active region corresponds to the time-walk curve. The time-walk is larger for hits with small charges (below 5 ke^-) and therefore these hits are detected late and assigned to the following bunch crossing. This measurement combined with hit simulation provides an estimation of the fraction of late hits for four sample positions in the detector, depicted in Figure 4 on the right. It shows that while SYNC and DIFF are comparably fast, LIN is the slowest one, with the largest fraction of late hits.

To mitigate this effect a design modification of LIN was proposed. Two diode-connected transistors, initially introduced to minimise the static current consumption at the output of the discriminator, were actually forcing other transistors to operate in the deep sub-threshold regime, and consequently making them slower. By removing those transistors a significant improvement in time-walk at the cost of a marginal increase in static current consumption was achieved [7]. Circuit simulations were used to estimate the time response of original and improved LIN and the corresponding expected fraction of late hits was computed. The new LIN shows a significantly lower fraction of misassigned hits, as shown in Figure 4 (right). The method was validated by matching the simulation of the LIN implemented in RD53A against measurements.

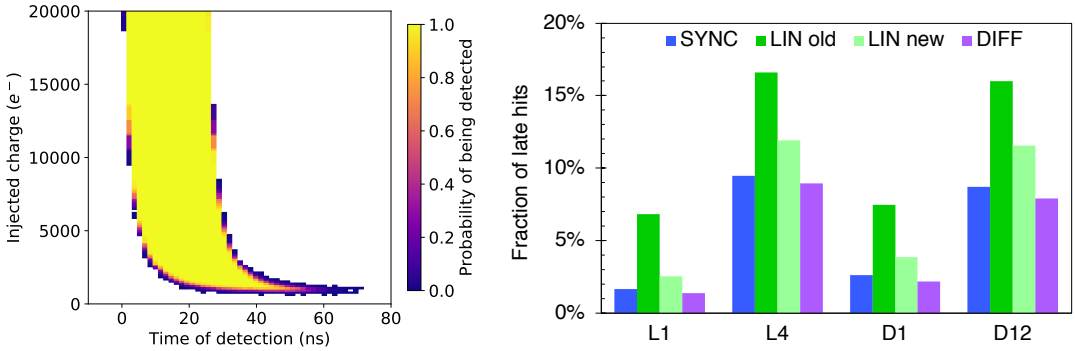

Figure 4: Example of the time response versus injected charge for original LIN (left) and the fraction of late hits for four positions in the detector: namely the first (L1) and last (L4) barrel layer and the first (D1) and last (D12) endcap disc (right).

7. Conclusion

During an extensive evaluation campaign, all three AFEs demonstrated strong points, and also limitations. The saturation of the preamplifier discharge current DAC of DIFF barely allows this AFE to discharge an equivalent input charge of 6 ke^- in two clock cycles, which would imply to operate at the limits of TOT response required for the innermost layer. SYNC appears to be the noisiest AFE: when connected to a sensor, the number of noisy pixels reaches 1.2 % with "slow discharge" settings and 3.8 % at "fast discharge". Moreover the noise occupancy after masking remains above the 10^{-6} requirement, which makes this front-end incompatible with the operation in the innermost layer of the CMS tracker. LIN was the slowest of the three AFEs, causing a misassignment of 6.8 % of hits in the innermost layer, while for the two other AFEs the fraction is below 2 %. However, for this AFE an improved design was developed and is expected to cause a 2.5 % misassignment rate in layer 1. Consequently, the linear front-end has been identified as the lowest risk option for the CMS final pixel chip.

References

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