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A Fault-tolerance Readout Network for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC

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We present a distributed, self-organizing and fault-tolerance readout network for the high-density electrode array targeting neutrinoless double-beta decay search in TPC. To realize a ton-scale high-pressure gaseous TPC, approximately 1×10^5 single-electrode Topmetal-S sensors need to be laid on a meter-sized plane. To readout those sensors, each sensor will integrate a router, and a 2D-Mesh network is formed by establishing local connections among nearby sensors. Each sensor not only generates and transmits its own data, but also forwards its nearby sensor's data, and data packets are finally received by a computer which is connected to the edge of the network. To avoid the faulty sensors to disable large parts of the network, a routing algorithm called Fault Tolerance XY (FT-XY) is implemented. A single router and a 10×10 network has been verified and tested on FPGA. The test result shows that the throughput of this network has reached 368.4Mbit/s Then the router is implemented on a 130 nm CMOS process.

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1. Introduction

Neutrinoless double beta decay (0νββ) is one of the most important frontier topics in particle physics. The discovery of neutrinoless double beta decay would confirm the Mayorana nature of neutrino [1]. The current experimental limit on the 0νββ half-life is set by KamLAND-Zen for ^{136}Xe to be more than 1.07×10^{26} years [2]. Therefore, experimental limits demand a future experiment at ton-scale with percent level or better full-width-half-maximum energy resolution. Among the current and planned experiments of 0νββ, the high-pressure gaseous Time Projection Chamber(TPC) [3,4] has the best potential of fulfilling all requirement for a next-generation 0νββ experiment when scaled up and stand out for excellent energy resolution, very low radioactive background level and good scalability. A pixelated charge readout plane will be used to measure the energy and tracks of a 0νββ event in high-pressure gaseous TPC. Moreover, high position resolution can be maintained with an appropriate charge readout scheme for gaseous TPC to further suppress the background through ionization imaging. Based on a 0.35um CMOS process, a low noise sensor named *Topmetal-S* [5], is being developed to meet the energy resolution requirements even without gas gain. Since 0νββ tracks are extended to tens of cm in length in high-pressure gas, *Topmetal-S* is designed to have mm-sized charge collection electrode, followed by a Charge Sensitive Amplifier (CSA), an internal ×2 buffer, a 3rd-order Sigma-Delta Analog-to-Digital Converter (ADC) and a digital decimation filter in the first prototype. *Topmetal-S* sensors will be laid on the charge readout plane in hexagonal pattern at a pitch no more than 10mm. Focusing electrode with hole-pattern matching the sensor array is placed above the array to improve the charge collection efficiency. However, to realize a ton-scale high-pressure gaseous TPC, approximately 1×10^5 *Topmetal-S* sensors would be laid on a meter-sized plane. The greatest challenge is a reliable high-density sensor readout and sensor control. It is practically impossible to route all data channels and control channels directly from each sensor to the edge of the plane. It is also difficult to guarantee air tightness by drawing high density channels out of the TPC.

In this paper, a distributed, self-organizing and fault-tolerance readout network is presented to realize readout of these sensors. The remainder of the paper is organized as follows: Section 2 describes the design of network, including the routing algorithm(FT-XY) of network and the design of router. The verification of a single router and a 10×10 network on FPGA is presented in section 3. The implementation of router chip is presented in section 4. Section 5 summarizes the paper.

2. Design of Network

To realize the high-density electrode array readout, the proposed scheme forms a sensor network by establishing local connection between nearby sensors. Based on the placement of 1×10^5 sensors on the plane, 2D-Mesh topology is adopted in the network. These hexagonal pattern placed sensors can be divided into two separated 2D-Mesh, the size of each one is about 224×224. As a node of the network, Topmetal-S will integrate a router. Each sensor not only generates and transmits their own data, but also forwards data from nearby sensors, and data packet is finally output though 224 row edge nodes, which are then received by a computer that is connected to the edge of the network. Therefore, a sensor consists of two parts: detector and router. The detector part includes a mm-sized charge collection electrode, a CSA, an internal ×2 buffer, a 3rd-order Sigma-Delta ADC and a digital decimation filter. The router part is used to

transmit its own data generated by the detector part or forward data from nearby sensors. The sample frequency and effective number of bits of the ADC after the digital decimation filter is 400 KHz and 14bits, respectively. Each hit sensor in every double-beta decay event will output about 50 ADC sampled data. According to physical simulation analysis, there are about 1000 double-beta decay events per second, and about 300 sensor nodes in this network will be hit by an event. Thus, the data transmission latency of the two 2D-mesh network should be no more than 1ms. The throughput of the two 2D-mesh network should reach 210 Mbit/s (14 bit/Sample × 50 Sample/node × 300 nodes/event × 1000 events/sec). In the best case (300 hit sensor nodes distributed in 300 rows), the throughput of a router should reach 700 Kbit/s (210 Mbit/s / 300 edge output nodes). In the worst case (244 hit sensor nodes distributed in a same row), the throughput of a router should reach 156.8 Mbit/s (14 bit/Sample × 50 Sample/node × 224 nodes/event × 1000 events/sec / 1 edge output node). Fault tolerance should be built into the network so that failed sensors will not disable a large section of the network.

2.1 Routing algorithm of network

In order to design fault-tolerant routing algorithm, the concept of fault block is introduced. The faulty block is defined as follows: All nonfaulty nodes are safe initially. A nonfaulty node is changed to unsafe if it has one or more faulty neighbors. Figure 1(a) shows three sample faulty blocks where gray nodes are faulty, green are unsafe, and other nodes are safe. The boundary rings are shown in boldface.

The routing algorithm of the network called Fault Tolerance-XY (FT-XY) is extended from regular-XY routing algorithm. Regular-XY consists of two phases: at the first phase, packets will be routed in y dimension till reduce Δy to zero, in the second phase packets are routed in x dimension until reduce Δx to zero. The FT-XY routing follows regular-XY routing (and the packet is in a "normal" mode) until the packet reaches a boundary node of a faulty block (this block is called routing block). At that point, the packet will be routed around the block (and the packet is in an "abnormal" mode) clockwise. Three routing path examples (from source node to destination node) are shown in figure1 (b). Path 1 (from S1 to D1) shows the situation when there are no fault nodes.The routing is the same as regular-XY routing:first reduce Δy to zero, then reduce Δx to zero. Path 2 (from S2 to D2) shows the situation when both X and Y directions have failed nodes. The packet routes around the block clockwise to reduce Δy to zero (M1) and then routes around the block clockwise to reduce Δx (M2), then in normal mode continue to reduce Δx to zero (D2). Path 3 (from S3 to D3) shows the situation when X directions have failed nodes. The Δy of the packet is already zero at the beginning. So the packet try to reduce Δx at first, then routes around the block clockwise to continue reduce Δx, then in normal mode to reduce Δx to zero (D3).

Figure 1: (a) example of faulty blocks (b) fault-tolerance routing

2.2 Design of router

The router can transfer data in five directions, each with two ports (input port and output port), as shown in the white part of Figure 4 (a). Local ports are used to exchange data with the

detector part, the other ports such as east, south, west and north ports are used to communicate with nearby nodes. In order to save cache, wormhole switching technology is adopted in the network, which is based on a flit level pipeline instead of a complete packet. Each packet is first divided into multiple flits, and then the router transfers the flit units without storing and forwarding the entire packet. Because the sensors will be assembled densely on PCB, the number of available paths on the PCB board used for communication between router ports are limited. Therefore, except for the local ports, each port of the router adopts Universal Asynchronous Receiver/Transmitter (UART) serial communication protocol. In order to improve the efficiency of the serial transmission, each flit contains two output data of ADC and two extra bits representing the type of flit (Header, data or Tail). Thus, the width of each flit is 30 bits. Once the sensor is hit, 25 flits will be generated, which will then be stored in the FIFO of the local input port. According to the requests from 5 input port FIFOs (included FIFO and UART_RX), the packet is transferred to the Routing Table (lookup) module by Arbiter module which adopts round robin policy. Then, the output direction for packets are decided by the Router Table(lookup) module according to the router's local information. Finally, the packet will be serially forwarded to nearby sensor or sent to the local output port.

3. Verification of single router and network on FPGA

In order to verify the function and performance of router and network, a single node and a 10×10 network had been built on a KC705 development kit. The block diagrams of a single router and a 10×10 network verification system are shown in Figure 2 and Figure 3, respectively. In these systems, PC not only generates test packets but also analyzes the received data packets. The 10G Ethernet TCP/IP protocol is used to communicate with PC in these systems.

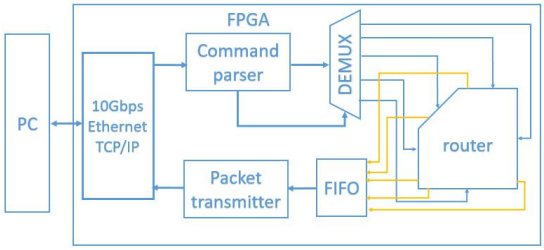


Figure 2: The block diagram of single router verification system on FPGA

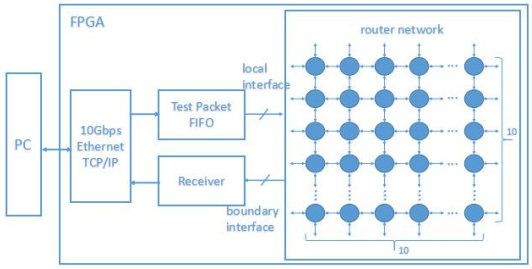


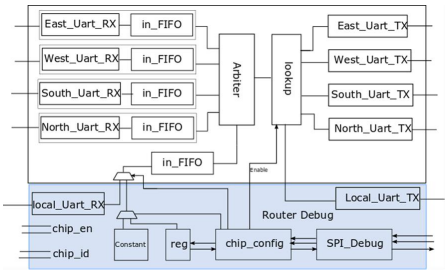
Figure 3: The block diagram of 10×10 network verification system on FPGA

In single router system, the command parser module receives data from Ethernet, and then sends packet to destination port combining with de-multiplexer module. Packets from 5 output ports of router are written into FIFO module first. Then the packet transmitter module reads data from FIFO and packs it to Ethernet unit. In the 10×10 network system, Test packet FIFO module receives data from Ethernet and then sends the data to a node in the network through the local input port of a router. The receiver module will receive the data packets at the network boundary nodes and send them to the Ethernet module. In these systems, when the router is

working at 50MHz, the throughput of a router reach to 36.84Mbit/s. The maximum throughput of a 10×10 network is 368.4 Mbit/s. And the maximum throughput of the network increases with the increase of network clock frequency and network scale. Therefore, even if the network size reaches 224×224, the router and network can meet the requirements.

4. The implementation of router chip

The router chip has been designed with a 130nm CMOS process. A block diagram and the layout of router chip is shown in Figure 4, which consists of two parts: router module and debug module. In order to make the router test easier, the router debug unit is designed to imitate the detector part of sensor and configure the router. Through SPI interface, the data source of local input port can be selected from local serial receiver, data packets configured by the debug unit, or constant packet. And the state of router can be configured to unsafe, safe or fault to imitate the situation of failed node.Post layout simulations show that the router can work up to 100MHz. The corresponding throughput of a router chip can reach 73.68Mbit/s.



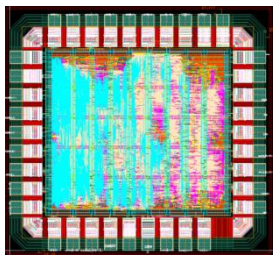


Figure 4: (a) The block diagram of router chip (b) The layout of router chip

5. Conclusion

For the readout of high-density electrode array, we have proposed a distributed, self-organizing and fault-tolerant readout network. The design of network, the verification of a single router and a 10×10 network on FPGA, and the router chip implementation are presented. A distributed, fault-tolerant routing algorithm FT-XY is implemented in this network. The verification result shows that when the router is working at 50MHz, the throughput of a router is 36.84Mbit/s and the maximum throughput of a 10×10 network is 368.4 Mbit/s. The post layout simulations on a 130nm CMOS process show that the router chip can work up to 100MHz.

Acknowledgments

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