PROCEEDINGS OF SCIENCE

Upgrade of the CSC Muon System for the CMS Detector at the HL-LHC

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The Large Hadron Collider (LHC) will be upgraded in several phases to significantly expand its physics program. After the current Long Shutdown 2 (LS2) from 2019-2020, the accelerator luminosity will be increased to 2-3$\times 10^{34}$cm^{-2}s^{-1}, exceeding the design value of 1×10^{34}cm^{-2}s^{-1} and allowing the CMS experiment to collect approximately 100 fb^{-1} per year. A subsequent upgrade during Long Shutdown 3 (LS3) from 2024-2026 will increase the luminosity up to 7.5×10^{34}cm^{-2}s^{-1}. The CMS muon system must sustain a physics program after LS2 that maintains the sensitivity to electroweak scale physics and TeV-scale new particle searches that has been achieved at lower luminosities. For the Cathode Strip Chamber (CSC) muon detectors, the electronics are being upgraded to handle the expected higher rates. The design of the upgraded CSC electronics will be discussed as well as the status of the first phase of the electronics installation. In view of the operating conditions at HL-LHC, it is vital to assess the detector performance at high luminosity. Accelerated aging tests are being performed to study the behavior of the CSC detectors under conditions which are nearly an order of magnitude beyond the original design values. The status and results of this irradiation campaign will be presented.

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1. Introduction

The Cathode Strip Chamber (CSC) system is installed in the endcap regions of the Compact Muon Solenoid (CMS) muon system. At High-Luminosity LHC (HL-LHC), luminosity will increase up to $7.5\times10^{34}\text{cm}^{-2}\text{s}^{-1}$, with Level-1 Trigger rate increased to 750kHz and a trigger latency of 12.5μs [1]. This increase in luminosity poses some unique challenges requiring unique solutions. Longevity studies in which CSC modules were irradiated to the equivalent of 10 years of HL-LHC data-taking anticipate good performance during Phase-2; however, the electronic readout system would suffer data losses, especially at high pseudorapidity ($0.9 < |\eta| < 2.4$) due to increased chamber occupancy. These losses can be mitigated by 1) reducing dead time and accommodating increased trigger latency by incorporating digital pipelines to the front-end electronics; 2) increasing readout rates by expanding the output bandwidth of the data acquisition boards; and 3) upgrading the high voltage system to satisfy higher power requirements of the new readout system. New electronic boards will handle higher rate and chamber occupancy mainly with high speed optical links and more powerful processors.

2. The CSC System

The CSC system comprises of 540 total CSC chambers. Each endcap has 4 stations (each station at a different z-axis position along the detector) and each station has 2 to 3 rings of CSC chambers, where rings are in a plane perpendicular to the beam line. CSC chambers are labeled by whether they are located in the positive or negative z Muon Endcap, followed by station and ring number (ME$\pm$Station/Ring). Each CSC has 6 layers of anode wires and cathode strips that detect hits, the ionization signals as a muon transverses the chamber gas volume (FIG. 1). Reconstruction of a muon track segment is made from 6 reconstructed hits. Chambers operate with a gas mixture of 40% Ar, 50% CO_2, and 10% CF_4. [4]

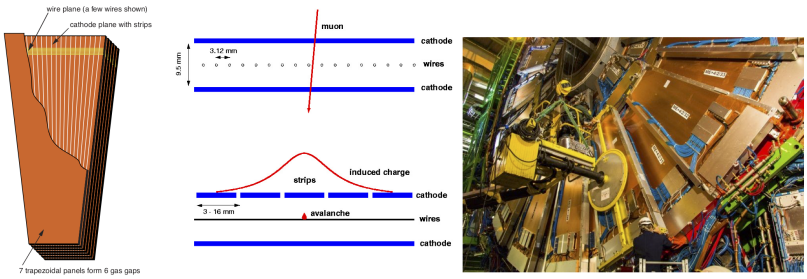

Figure 1: Cathode Strip Chamber (CSC) and CSC installed on disk

The CSC system is part of the CMS Muon Detector (FIG. 2) and, together with Drift Tube (DT) chambers, Resistive Plate Chambers (RPC), and Gas Electron Multiplier (GEM) detectors, gives high redundancy for robust muon triggering and reconstruction in CMS [2]. Features of the CSC system include precise measurements of muon azimuthal position (< 200 μm per CSC), as well as good timing resolution (< 3.5 ns per segment), and the ability to handle high particle rates. The chambers can also operate in non-uniform magnetic fields.

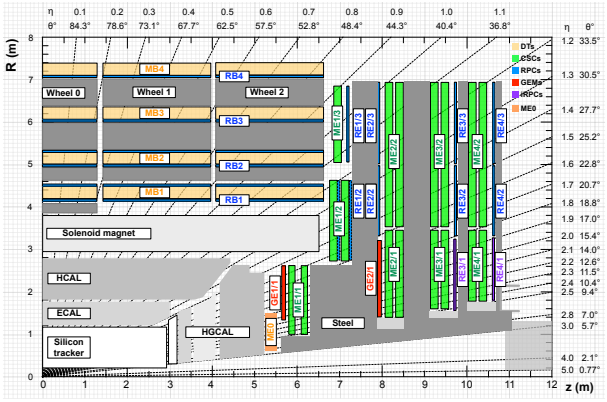

Figure 2: CMS muon system cross section. The Phase-2 CSC Upgrade will be in the high pseudorapidity region, or the inner rings

3. Electronics Upgrade

Data projections show a 10% event loss rate at a 750kHz rate of accepted events that pass the CMS Level-1 (L1) Trigger (FIG. 4). New boards are designed to handle higher rate and chamber occupancy by utilizing high speed output optical links and more powerful processors. The main upgrades to the CSC electronics system (FIG. 3) are outlined below.

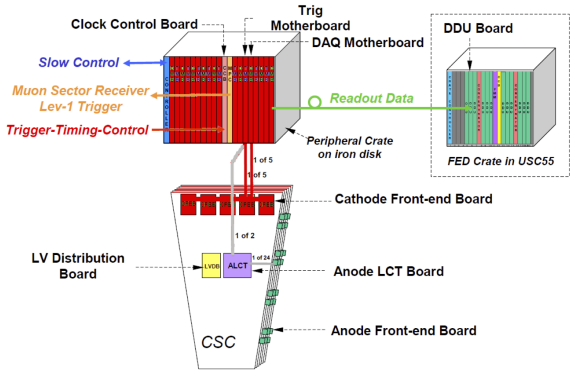

Figure 3: CSC Electronic System

- Digital Cathode Front-End Board (DCFEB): Flash ADCs which digitize and store analog signals will be used, instead of switch capacitor arrays on CFEB, the predecessor to the DCFEB (FIG. 5). The FPGA which stores digitized signals from the ADCs will be upgraded from Virtex I to Virtex 6. An optical readout will replace the copper cabling based readout. ME1/1 DCFEBs installed during LS1 will be removed and installed on the ME234/1 inner rings, and new xDCFEBs, modeled on the DCFEB, will be installed on ME1/1. xDCFEB will mitigate risks associated with PROM longevity due to radiation at HL-LHC with the addition of a remote programming option for the FPGA through the GBTx.
- Anode Local Charged Track Board (ALCT): The FPGA will be upgraded from Virtex E to Spartan 6 to handle increased Level-1 Trigger Accept (L1A), the signal sent from the

L1 Trigger to the front-end electronics to start the readout [3], latency due to the longer processing time period required for the new CMS track trigger to accept events.

- Optical Trigger Motherboard (OTMB): The copper readout will be upgraded to optical links and the FPGA will be upgraded.
- Optical Data Acquisition Motherboard (ODMB): The optical DMB will have higher bandwidth optical links to the Front-End Driver (FED) system. Via optical links, firmware and parameters can be transmitted to the front-end boards. The previous ODMB used one link running at 1.6 Gb/s. Each new link to the FED will run at 12.5 Gb/s, providing a bandwidth to the FED of up to 50 Gb/s over 4 links. FEDs will also be replaced to accept higher input rates.

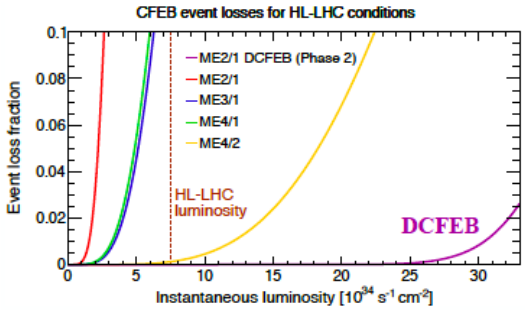

Figure 4: CFEB and DCFEB event loss for HL-LHC conditions. The dashed line is the anticipated luminosity at HL-LHC, below which CFEBs in ME234/1 will experience event loss. DCFEBs perform well-above this luminosity.

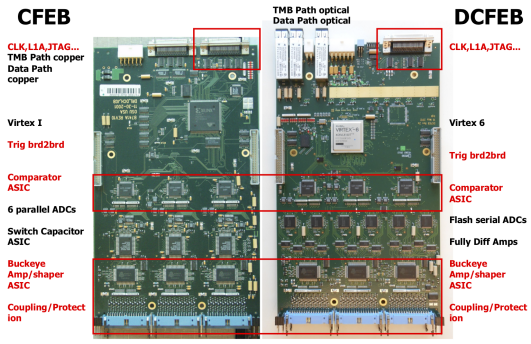

Figure 5: Cathode Front-End Board and Digital Cathode Front-End Board comparison

4. Longevity Studies

CSC longevity studies and performance measurements under HL-LHC background conditions were performed at CERN GIF++ with an intense ^{137}Cs source and muon beam. Basic chamber characteristics were monitored during the irradiation, and the CSC muon detection performance as a function of the accumulated charge was measured during the beam tests. The longevity studies

were performed at the baseline expected HL-LHC luminosity of $5\times10^{34}\text{cm}^{-2}\text{s}^{-1}$. The accumulated charge at the test is 3 times larger than the expected total integrated charge accumulated during the HL-LHC for chambers with the highest expected fluence (ME1/1 and ME2/1). Results for ME1/1 are shown. Relative current (FIG. 6) and spatial resolution (FIG. 7), evaluated as a standard deviation of predicted hit position from measured position, were stable against the growth of integrated charge. No significant change in chamber performance was observed during the test.

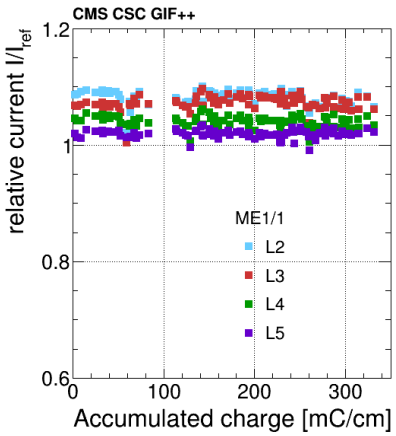

Figure 6: Relative currents of the irradiated layers (L2-L5) in ME1/1 at HL-LHC luminosity of $5\times10^{34}\text{cm}^{-2}\text{s}^{-1}$. Relative currents are stable.

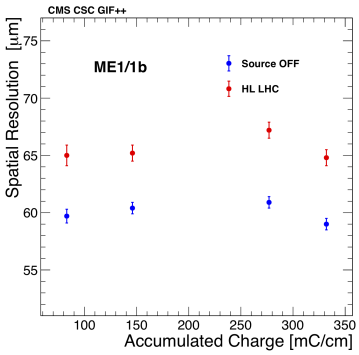

Figure 7: Spacial resolution of ME1/1 as a function of accumulated charge without additional background and with the equivalent average background occupancy at HL-LHC luminosity of $5\times10^{34}\text{cm}^{-2}\text{s}^{-1}$. Spatial resolution is stable.

5. CSC Upgrade Timeline

The upgrade of the CSC system will continue through LS3. During LS1, ME1/1 CFEBs were replaced by DCFEBs, and an additional 72 ME4/2 chambers were added to the CSC system. The ME1/1 and ME4/2 anode FPGAs were upgraded and data and trigger motherboards for DCFEB readout were upgraded to optical. Currently in LS2, ME1/1 DCFEBs are being replaced by xDCFEBs, while DCFEBs from ME1/1 are being moved to ME234/1. The anode trigger boards are

also upgraded with optical readout and upgraded FPGAs, and there is a new optical trigger motherboard. For LS3, there will be a new optical data motherboard and back-end driver system to accommodate higher input rates.

6. Conclusion

The CSC muon system of the CMS detector is being upgraded in order to handle the higher data rates of the HL-LHC. During LS2, on-chamber electronics are being installed on eight rings of the CSC muon system. Electronic board production is in progress with current completion of xDCFEBs: 60% and ALCTs: 70%. One ring of 36 chambers (ME-1/1) is completely refurbished and reinstalled. Currently, a second ring of 18 chambers (ME-2/1) is being refurbished. 6 additional rings will be refurbished by 2020.

References

[1] CMS Collaboration, *The Phase-2 Upgrade of the CMS Muon Detectors*, Technical Report CMS-TDR-019, 2017.

[2] CMS Collaboration, *CMS Physics Technical Design Report Volume 1: Detector Performance and Software*, Technical Report CERN-LHCC-2006-001, CMS-TDR-8-1, 2006.

[3] CMS Collaboration, *The Phase-2 Upgrade of the CMS Level-1 Trigger - Interim Report to the LHCC*, Technical Report CERN-LHCC-2017-013. CMS-TDR-017, 2017.

[4] CMS Collaboration *The CMS Muon Project*, Technical Report CERN-LHCC-97-032, CERN, 1997.

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