

The design and layout of the Phase-II upgrade of the Inner Tracker of the ATLAS experiment

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In the high luminosity era of the Large Hadron Collider (HL-LHC), the instantaneous luminosity is expected to reach unprecedented values, resulting in about 200 proton-proton interactions in a typical bunch crossing. To cope with the resultant increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk), aiming to provide tracking coverage up to $|\eta| < 4$. The Technical Design Reports for the strip and pixel subsystems were published in 2017 and 2018, respectively. Since their publication, the ITk design has undergone further refinement, in particular for the pixel subsystem, addressing the then-pending design choices in several areas and accommodating updated engineering requirements. In addition, the simulation model of the detector has become more realistic, leading to updated estimates of the material budget. In these proceedings an overview of the updated layout is presented and the resultant expected tracking performance discussed.

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1. Introduction and Motivation

Precision studies of the Standard Model (SM) and the search for physics Beyond the Standard Model (BSM) are the goals of the ATLAS experiment [1] at the Large Hadron Collider (LHC). By the end of Run 3, currently scheduled for 2023, the integrated luminosity is expected to reach 300fb^{-1} [2]. The High-Luminosity LHC (HL-LHC) will allow ATLAS to collect up to 4000fb^{-1} of integrated luminosity within 10 years, starting from mid-2026, thereby significantly increasing its sensitivity to BSM physics in precision measurements and searches [3, 4]. Rising to $\mathcal{L} = 7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, the instantaneous luminosity will yield an average number of $\langle \mu \rangle = 200$ proton-proton interactions per bunch-crossing (pile-up) [2]. The current Inner Detector (ID) of ATLAS, composed of a silicon pixel, a silicon strip and a Transition Radiation Tracker (TRT), is designed for radiation doses reached at integrated luminosities from 400fb^{-1} to 850fb^{-1} and will not be able to cope with the HL-LHC radiation doses [2, 4]. Thermal runaway due to an increase in leakage current would occur with the present cooling system, irrespective of the power-supplies not being able to provide the corresponding currents and the hit efficiencies would be too low for the tracking requirements. Furthermore, the present granularity would not suffice to resolve the higher track density due to the larger pile-up, thus decreasing the precision of measurements and reach of searches. Finally, the track density would lead to saturation of the bandwidth between on-detector and off-detector read-out units and the TRT would reach 100% occupancy, both resulting in lost hits. Given the aforementioned reasons, it was decided to replace the ID by the Inner Tracker (ITk). In contrast to the ID, the ITk will be an all-silicon tracking detector [4]. It will cover¹ 2π in ϕ and $|\eta| < 4$, compared to the ID, which covers $|\eta| < 2.5$ [1, 2].

The design requirements of the ITk at the HL-LHC can be summarised as: tracking quality at least as good as the present ID [5]; radiation tolerance of $1.31 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$ for the pixel and $1.2 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ for the strip detector; hit densities of up to $0.643 \text{hits}/\text{mm}^2$ for the pixel and $0.005 \text{hits}/\text{mm}^2$ for the strip detector; trigger rates of 1 MHz to 4 MHz with up to $35 \mu\text{s}$ latency [2, 3, 6]. The last point is essential for a new hardware-based track-trigger planned with the ITk, employed to reduce trigger background rates in the Level-1 trigger system [4].

This paper describes the most recent layout and design of the ITk in Sections 2 and 3. The resulting tracking performance is presented in Section 4.

2. The Pixel Detector

Unless indicated otherwise, this section follows Ref. [3]. The latest geometry of the ITk is shown in Figure 1a. It depicts one quadrant of the ITk and the pixel detector is colored in red. The ITk is divided into a barrel, consisting of concentric layers around the beam-pipe, and two end-caps made of discs, one on each side of the barrel [2]. Since the Technical Design Reports [2, 3], changes in the geometry of the pixel and strip detector (see Section 3) have been made, resulting from the decisions to: install a High Granularity Timing Detector (HGTD) [7] in both end-caps, shortening the ITk by 15 cm on each side; provide space for cables and cooling; optimise the material budget; simplify the installation of components [8].

¹With the x -axis pointing to the centre of the LHC, the y -axis towards the sky, the z -axis along the beam-pipe and corresponding spherical azimuthal angle ϕ and inclination angle θ , the pseudo-rapidity η is defined as $\eta = -\ln(\tan(\theta/2))$.

In the pixel detector, the combination of a sensor, one or four bump-bonded read-out chips and a glued flexible Printed Circuit Board (PCB) electrically connected via wirebonds (25 μm diameter bare aluminium wires), is called a module. The pixel detector powers its modules in series, reducing the material budget, but requiring AC-coupling of data lines due to a missing common ground. Modules with two read-out chips per sensor, as presented in the Technical Design Report [3], are not foreseen any more [8].

Planar and 3D (only innermost layer) sensors will be used and pixel sizes of 50 $\mu\text{m} \times 50 \mu\text{m}$ and 100 $\mu\text{m} \times 25 \mu\text{m}$ are under consideration. 3D sensors have electrodes penetrating the entire depth as shown in Figure 1b. The pillar-like electrodes allow for full depletion at smaller voltages compared to the planar type, also after large irradiation, yielding less power dissipation.

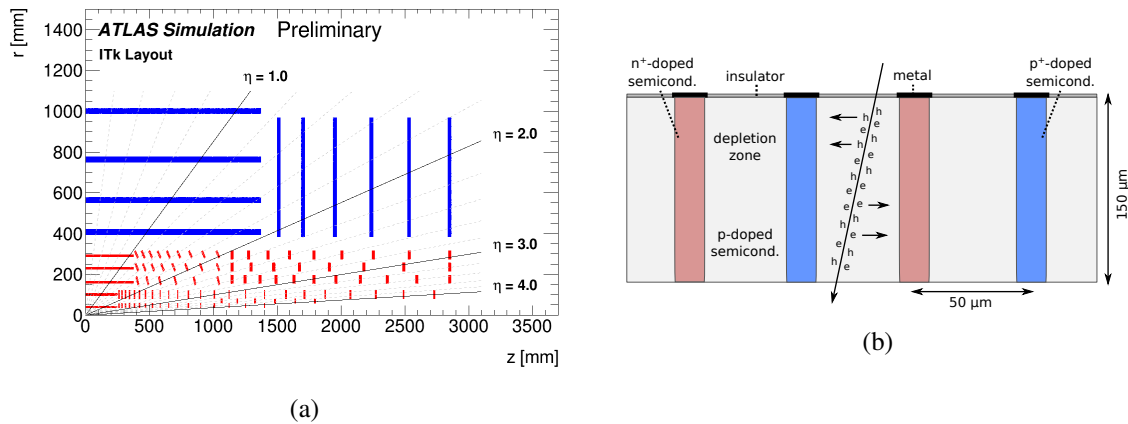


Figure 1: (a) A quadrant of the most recent design of the ATLAS ITk [8], and (b) cut-away view of a 3D-pixel sensor.

For read-out, the ATLAS ITkPix chip, a variation of the RD53a [9] will be used. Built in a CMOS process with 65 nm-sized features, it offers $400 \times 384 = 153\,600$ pixels, while covering 2 cm \times 2 cm. Each pixel comes with a 4-bit Time-over-Threshold (ToT) to quantify the amount of charge deposited by a penetrating particle. Protection from bit flips (Single Event Upsets) in the chip's registers is provided by a triple redundancy mechanism and a continuous reconfiguration of a chip during operation, similar to what is employed by the ATLAS Insertable B-Layer (IBL) [3, 10].

Radiation doses up to 2 to 3 $\times 10^{16}$ n_{eq}/cm² are expected for the innermost layer. Limited by the available technology within the time constraints, it was decided to replace the innermost two pixel layers after about half of the radiation dose has been acquired (2000 fb⁻¹). This corresponds to maximum doses of 1.31 $\times 10^{16}$ n_{eq}/cm² for the 3D sensors and 3.8 $\times 10^{15}$ n_{eq}/cm² for the planar ones, at which hit efficiencies of > 97% are targeted. Test-beam campaigns have shown that sensor prototypes fulfill these requirements, as shown in Figures 2a and 2b [11, 12]. Since no ITkPix prototype is available yet, the results presented were obtained using the ATLAS IBL FE-I4 read-out chip [13].

3. The Strip Detector

The strip detector is shown in blue in Figure 1a and changes in the geometry compared to

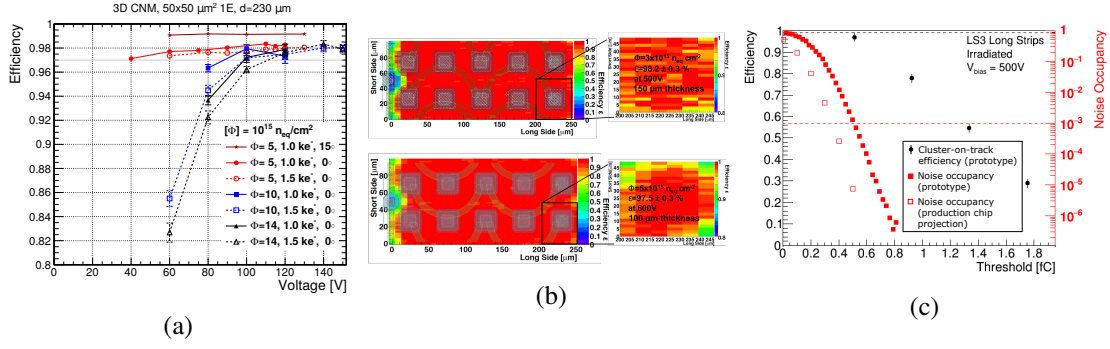


Figure 2: (a) Efficiency versus depletion voltage for a 3D pixel sensor at different fluences Φ , thresholds and incidence angles [3, 11], (b) position dependent color coded efficiencies for two planar pixel sensors of different thicknesses at different fluences and depletion voltages [3, 12], and (c) cluster-on-track efficiencies and noise occupancies of a strip module prototype and the projection of the noise occupancies to the production read-out chip [2].

the Technical Design Report [2], which this section follows, were discussed in Section 2. A strip detector module is composed of: a sensor; one to four hybrids, each consisting of a PCB hosting the read-out chips (ABCStar) and up to two input-output data management chips (HCCStar); a power-board with a DC-DC converter and a power-control chip (AMAC). The module geometry in the barrel is rectangular, while end-caps modules are isosceles-trapezium-shaped (see e.g. Ref. [2] for pictures and drawings). Functioning strip detector module prototypes are available.

Both barrel and end-caps use silicon strip sensors with strip lengths of 18.1 mm to 60.2 mm. In the barrel the strip pitch is 75.5 μm , while this is not uniform for the end-caps, due to the divergent sensor geometry. The used ABCStar read-out chip is built in a CMOS process with a 130 nm feature size and offers 256 binary read-out channels. Electrical connections between sensors, read-out chips and hybrid PCBs are established using wirebonds.

Intrinsically, strip detectors offer 2D position information. To obtain 3D position information with the ITk strip detector, each module has a partner, installed on the opposite side of the primary module support structure, rotated by a stereo angle of 52 mrad (40 mrad) in the barrel (end-caps).

Test-beam studies were conducted to ensure that the strip detector can withstand the anticipated radiation doses. Resulting efficiencies (black dots) and noise occupancies (filled squares) are shown in Figure 2c for a barrel prototype module irradiated to the end-of-lifetime dose of $8 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$. Also shown is a projection (open squares) of the noise occupancies to the expectation with the production read-out chip. While the range in which efficiency ($> 99\%$) and noise occupancy ($< 10^{-3}$) requirements can be fulfilled simultaneously with the prototype is narrow, the range for the production chip projection is wider. First test-beam studies with the production chip indicate that this is indeed the case after irradiation (end-caps module, $1.5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$), though investigations are on-going.

4. Expected Performance

The expected performance of the ATLAS ITk was studied in Ref. [8] for the layout presented

here. Figure 3a shows the simulated material budget as a function of η . Compared to Run 2, the maximum material budget is reduced from almost $6 X_0$ to less than $2 X_0$ [3]. The main reasons for this difference are lighter support structures and fewer cables due to e.g. serial powering in the ITk.

The Vertex Reconstruction and Selection (VRS) efficiency simulated for vector-boson-fusion $H \rightarrow 4\nu$ events as a function of the local pile-up density is shown in Figure 3b. These events are characterized by the presence of very forward jets and challenge the forward tracking capabilities of the ITk. Vertices are reconstructed using the Adaptive Multi-Vertex Finder algorithm [14] and selected according to the maximum $\sum p_T^2$ of vertex tracks. While the $H \rightarrow 4\nu$ VRS efficiency decreases for Run 2 as the local pile-up density increases, it is almost constant for the ITk for both pixel sizes. This shows that most of the interactions per bunch crossing are reconstructed at $\langle \mu \rangle = 200$ and that there are hardly any merged or overlapping vertices. A VRS efficiency of less than unity is expected for $H \rightarrow 4\nu$ events, as about 20% of them fail the maximum $\sum p_T^2$ [3].

The term b-tagging describes the identification of jets emerging from b -quarks. The expected ITk b-tagging light-jet rejection as a function of b-tagging efficiency is depicted in Figure 3c for $25 \mu\text{m} \times 100 \mu\text{m}$ pixels. Run 2 results are indicated by green crosses and should be compared to the dashed line representing the ITk restricted to the ID coverage, $|\eta| < 2.5$. A stronger light-jet rejection is expected with the ITk.

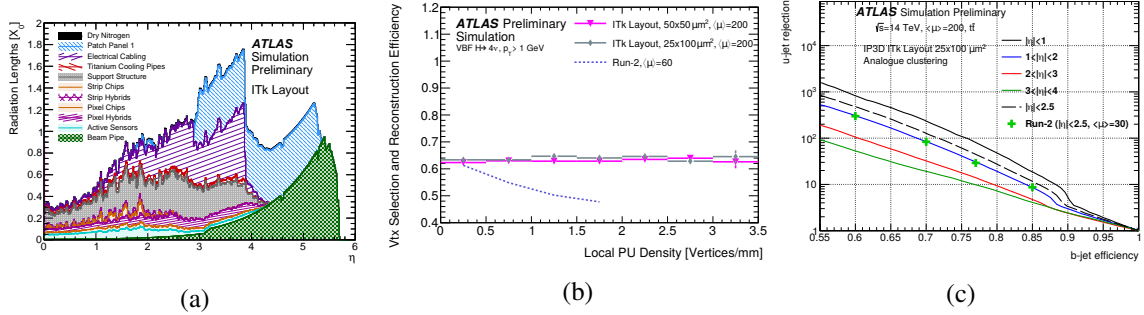


Figure 3: (a) ITk material budget in radiation lengths versus η , (b) vertex reconstruction and selection efficiency for $H \rightarrow 4\nu$ events, and (c) light-jet (u -jet) rejection versus b-tagging efficiency [8].

5. Summary

To cope with the radiation damage, track densities and trigger rates at the HL-LHC, the ATLAS ID has to be replaced by the ITk. Prototype results show that these requirements can be fulfilled. Simulation studies conclude that the ITk can maintain or exceed the current ID performance.

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