PROCEEDINGS OF SCIENCE

The CMS Tracker Upgrade for the High Luminosity LHC

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The LHC machine is planning an upgrade program which will smoothly bring the instantaneous luminosity to about $5-7.5\times10^{34}\text{cm}^{-2}\text{s}^{-1}$ in 2028, to reach an integrated luminosity of 3000 fb^{-1} and possibly up to 4500 fb^{-1} by the end of 2039. This High Luminosity LHC scenario, HL-LHC, will require an upgrade program of the LHC detectors known as Phase-2 upgrade. The current CMS Outer Tracker, already running beyond design specifications, and CMS Pixel Detector will not be able to survive HL-LHC radiation conditions and CMS will need completely new devices, in order to fully exploit the highly demanding conditions and the delivered luminosity. The new Outer Tracker should also have trigger capabilities. To achieve such goals, R&D activities have explored options for both the Outer Tracker and for the Inner Tracker. The solutions developed will allow to include tracking information in the first trigger stage. The design choices for the Tracker upgrades are discussed along with some highlights on technological approaches and R&D activities.

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1. Introduction

The High Luminosity Large Hadron Collider (HL-LHC) program [1] is going to last nearly 10 years operating at $5-7.5\times10^{34}\text{cm}^{-2}\text{s}^{-1}$ instantaneous luminosities, with an average number of 140-200 simultaneous inelastic proton-proton collisions per bunch crossing, targeting a total integrated luminosity between 3 and 4.5 ab^{-1}. The present CMS tracker [2] (Phase-1 Tracker) cannot sustain the resulting data rates and radiation levels and has to be completely replaced. Among the requirements for the new CMS tracker [3] for the HL-LHC (Phase-2 tracker) are: enhanced radiation tolerance, sustaining a Total Integrated Dose (TID) up to ten times larger, the ability to participate in first level trigger (L1) decisions, compliance with the extended 12.5 μs L1 latency, higher data rate capability (L1 accept rate up to 750 kHz), higher granularity in order to keep the channel occupancy below 1%, extended tracking coverage (up to $|\eta|=4$) and reduced material budget for improved tracking performance. Figure 1 shows the longitudinal layout of one quarter of the CMS Phase-2 Tracker. It is divided into the "Inner Tracker" (IT) in the region closest to the beam line, composed of hybrid silicon pixel module detectors, and the "Outer Tracker" (OT) in the outer region, featuring detector modules with silicon sensor doublets.

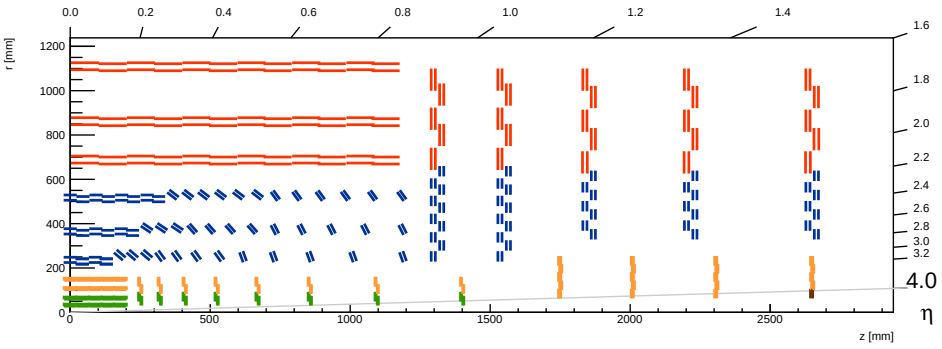

Figure 1: Layout of one quarter longitudinal section of the CMS Tracker for the HL-LHC. In green (yellow) the silicon pixel detectors of the Inner Tracker with two (four) readout chips per module. In blue (red) the PS (2S) silicon detector modules of the Outer Tracker (see main text for details).

2. The Inner Tracker

The IT is composed of about 3900 hybrid pixel modules, covering a total surface of 4.9 m^2 and featuring around 2 billion readout channels, more than 16 times the present CMS Phase-1 pixel detector. Two types of modules are used, with either 1×2 or 2×2 readout chips (ROC), organised into four barrel layers (TBPX) plus eight small disks (TFPX) and four large disks (TEPX) per end. Half-cylinders hold the various sub-parts and their services, allowing detector removal for maintenance during LHC shutdowns. In addition to extending the tracking acceptance up to $|\eta|=4$, the four large TEPX disks at either end of the detector are used to perform real time luminosity measurement. For this purpose their modules receive extra luminosity triggers at 75 kHz (and up to 10 MHz in the absence of normal data-taking). The innermost rings of the outmost TEPX disks are exclusively used for beam background and luminosity measurements.

An extensive R&D program is ongoing to develop silicon sensors capable to maintain sufficient charge collection efficiency in the harsh HL-LHC radiation environment. The inner layer (sitting at just 3 cm distance from the beam line) have to sustain a TID of about 1.2 Grad and a fluence of $2.3 \times 10^{16}\,n_{eq}/cm^2$ in 10 years of HL-LHC operation. Thin planar n-in-p sensors, with $100-150\,\mu$m active thickness, are considered for this scope. A possible alternative choice for the inner TBPX layers and the inner TFPX rings are 3D sensors, which feature a better radiation resistance and require lower bias voltages, at the cost of enhanced cell capacitance and a more complex fabrication process. A review of recent studies is reported elsewhere in this conference [4]. Two possible pixel aspect ratios ($25 \times 100\,\mu m^2$ and $50 \times 50\,\mu m^2$) are considered; a small cell size is needed in order to keep occupancy below 0.1%.

A chip with adequate radiation hardness and featuring low noise front-end electronics is needed to read out the relatively small signals provided by thin silicon sensors. The RD53 Collaboration [5] is developing the ROC for both the ATLAS and the CMS Phase-2 inner tracker detectors. The chip design is realized in 65 nm CMOS technology, featuring $50 \times 50\,\mu m^2$ elementary cell, low-threshold (below 1000 e), high hit and trigger rate capability (one 160 Mb/s input link and up to four 1.28 Gb/s output links) and support for the serial powering scheme. Design concepts have been recently demonstrated by RD53A, a half-size chip prototype, which has been successfully tested up to 500 Mrad. The chosen CMS final chip size is $16.8 \times 21.6\,mm^2$, featuring 336×432 cells. The submission of the first full size CMS chip prototype is expected in 2020.

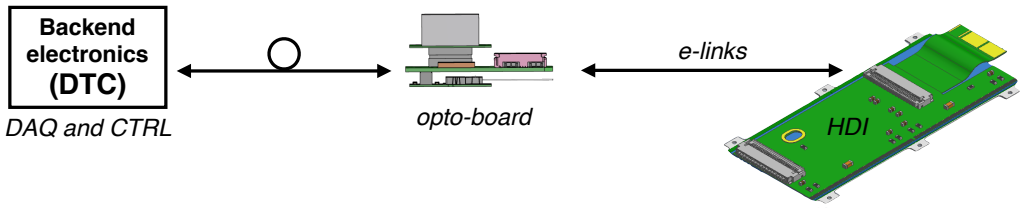

Figure 2: Sketch of the DAQ and control chain for the IT detector. Bidirectional high-speed, low-mass, electrical links (e-links) connect the readout chips of the module (via the HDI) to one opto-board which implements the optical link connections to the Data Trigger and Control (DTC) back-end system.

Each IT module consists of one silicon sensor bump-bonded to two (1×2 modules) or four (2×2 modules) readout chips. The electrical line of the sensor bias voltage and the readout chips are wire bonded to a flexible printed circuit, called High Density Interconnect (HDI), glued on top of the sensor and providing electrical connections to power services and to one *portcard*. Portcards are opto-boards which implement the optical links to the Data Trigger and Control (DTC) system. The links are based on the low-power GigaBit Transceiver (LpGBT) [8]; two LpGBT transceivers and two VTRx+ [9] optical link modules are hosted per board. The portcards are integrated in the half-cylindrical structures enclosing the IT, where radiation levels are sustainable for the components. Custom developed, AC-coupled, high-speed and low-mass electrical links (e-links), of the order of 1 m length, connect (via the HDI) the ROCs on each module to one portcard. In total up to six 1.28 Gb/s up-links per module are implemented, carrying all the module's data and monitoring information, and one 160 Mb/s down-link, bringing clock, trigger, commands and configuration data to the module.

3. The Outer Tracker

In order to exploit the high instantaneous luminosity, tracker information is used right in the L1 trigger decision, providing better muon p_T resolution, e-γ discrimination and particle isolation determination. An overview of the Phase-2 CMS L1 can be found in [6]. An FPGA-based *track-finder* system performs real-time patter recognition and track fitting, processing *stubs* sent out by modules at every LHC bunch crossing. Stubs are track segments reconstructed from correlated signals generated by particles in two closely-spaced silicon sensors within each OT detector module (see Fig. 3). A configurable acceptance window is used to select stubs corresponding to tracks with p_T exceeding 2 GeV. The correlation procedure is performed by the ASICs on the module.

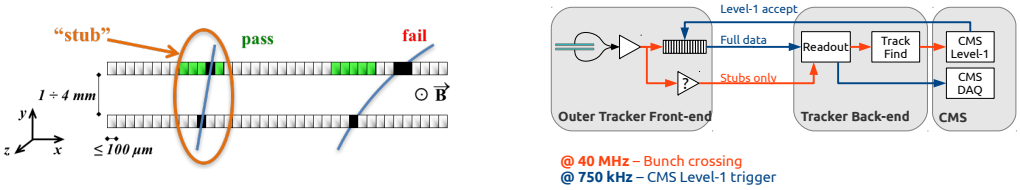

Figure 3: Left: the correlation of signals in closely-spaced sensors enables rejection of low-p_T particles; the channels shown in green represent the programmable selection window defining accepted stubs [3]. Right: illustration showing the 40 MHz stubs readout (in red) and the 750 KHz full tracker data readout upon L1 accept.

This approach is central to the design of the detector modules of the OT. The Strip-Strip (2S) modules (represented in red in Fig. 1), feature two silicon strip sensors; the macroPixel-Strip (PS) modules (blue lines in Fig. 1), feature one silicon strip sensor on top of one macropixel sensor (face closer to the beam line) which allows a fine determination of the z coordinate of track hits. Spacing between sensor pairs varies between 1.6 and 4.0 mm, depending on their geographical position, keeping homogeneous stub p_T thresholds. The OT provides L1 coverage up to $|\eta| \sim 2.5$. It covers an area of about 190 m^2 with 13296 detector modules, quantities not dissimilar to those of the present Phase-1 silicon strip tracker; the number of strips, however, is around four times larger (42 million), and 170 million macro-pixels add to this number, making the Phase-2 tracker a highly granular detector, with expected occupancy levels below 1%. An innovative tilted geometry is adopted for the inner barrel layers, which achieves a better trigger performance and also reduces the total number of PS modules, thereby reducing material budget and cost.

The OT modules have quite a complex design, which comprises several readout ASICs and auxiliary chips, implemented on flexible hybrid circuits. In 2S modules a total of 16 *CMS Binary Chips* (CBC) read out the microstrip sensors and perform the top-bottom correlations for track stub identification. They are implemented on two *Front End Hybrids* (FEH), on either side of the module. The *Concentrator Integrated Circuit* (CIC) ASIC receives and formats data to and from the readout ASICs, sending it to the Service Hybrid (SEH), where one lpGBT and one VTRx+ implement the link to the back-end DTC system. In addition, the SEH performs also bias voltage distribution to the sensors and power distribution to the ASICs. In PS modules, microstrips are read out by 16 *Short Strip ASICs* (SSA), located on two FEHs, while the macropixel readout is performed by 16 *Macro Pixel ASICs* (MPA), bump-bonded to the macropixel sensor. MPAs also

perform the stub finding. Optical links and Power distribution functions in PS modules are implemented on two separate hybrid circuits: the *Readout Hybrid* (ROH) and the *Power Hybrid* (POH) respectively.

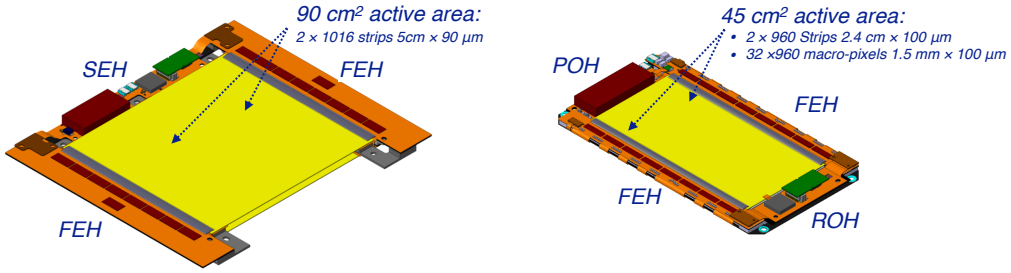

Figure 4: Left: CAD drawing of the 2S modules of the Outer Tracker, featuring two parallel silicon strip sensors, with two sets of 1016 strips 5 cm long with 90 μm pitch. Right: drawing of the macropixel-strip (PS) modules of the Outer Tracker, featuring one silicon strip sensor on top of one macropixel sensor. The strip sensor features two sets of 960 strips 2.4 cm long with 100 μm pitch. The macropixel sensor features 32 rows of 960 macropixels (1.5 mm $\times$ 100 μm).

4. Power distribution and cooling

Power distribution is going to be a major challenge for the Phase-2 tracker. The large increase of the total number of channels, the high data bandwidth, the additional logic required to provide tracking information to the L1 trigger and the low-noise, low-threshold analog circuits needed to read out signals from thin silicon sensors, all contribute to boost the IT and the OT power demand. Despite the adoption of newer 135 and 65 nm CMOS technologies, the power required by the Phase-2 tracker is more than three times that of the present Phase-1 tracker, summing up to about 50 kW for IT and 100 kW for OT. Integration constraints do not allow to increase the total cross section of the power cables outside the tracker; at the same time, in order to keep low the material budget inside the tracking volume, thin copper-clad Aluminum wires are used to distribute the power inside the tracker structure. As a result, the voltage drop across the power lines feeding each module greatly exceeds the voltage required (with strict tolerances) by the front-end electronics, making the direct voltage regulation from a remote power system problematic, even when sense-wire loops are adopted to detect load variations. Different power distribution schemes are thus required, which provide local voltage regulation inside the detector, allowing higher voltages at the output of the power supplies. Separate approaches are adopted for the OT and the IT.

In the OT modules a two-step conversion based on DC/DC converters (bPOL12V and bPOL2V5 [7]) is used to convert one voltage line into the voltage levels required by the front-end electronics (2.5, 1.2 and 1.0 V). The DC/DC conversion is implemented on the SEH for 2S modules and in the POH for PS modules. Each OT module is connected to one power supply channel and can be individually operated and monitored, making for a highly granular power system. The maximum power which can be provided to individual modules is limited by the voltage drop along the cables and by the operating voltage range of the bPOL12V DC/DC converter (6 - 11 V). Present plans foresee to power the modules through $\sim$ 60 m long cables, providing around 5.2 W (8.8 W) to 2S (PS) modules. Prototyping work is ongoing on all the components of the power chain.

Space occupancy, material budget and radiation resistance of the available DC/DC converters prevent their use in IT pixel modules. A serial powering scheme is therefore adopted for the IT. Modules are connected in series forming chains of up to 12 modules. One current source drives each chain, providing power to an effective voltage which is a multiple of the voltage drop across each module (see Fig. 5). Readout chips inside the same module share the current in parallel. Around 500 serial chains are needed to power the entire IT. Separate chains are formed for 2-chip and 4-chip modules, with maximum currents up to 4 A and 8 A, respectively. The serial powering scheme is supported by the ROC, by virtue of the Shunt-LDO (SLDO), a circuital element inside the chip which provides LDO (low-dropout linear regulation) functionality, ensuring local voltage regulation, and shunt functionality, decoupling the chip power demand from the current flowing across the chain. Separate SLDO, working in parallel, are used to power the analog and digital domains of the ROC. Serial powering is a relatively new technology in high-energy experiments, never used before in large scale applications. By construction, modules within each chain have separate local voltage references, which demands extra consideration in the integration of the system and in the distribution of bias to the silicon sensors, which follows a parallel scheme. An active R&D program is ongoing within the ATLAS, CMS and RD53 Collaborations. Serial chains with up to 16 RD53A chips have recently been successfully operated in bench tests.

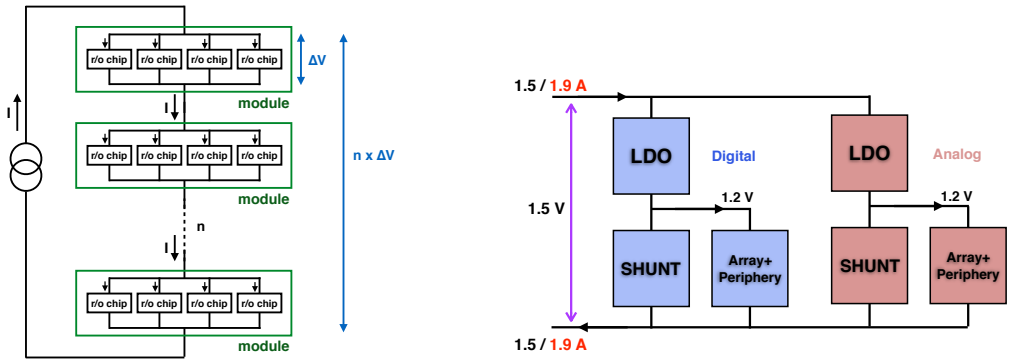

Figure 5: Left: the voltage drop across a serially powered chain composed of n modules is $n \times \Delta V$, where ΔV is the voltage drop across each module. Readout chips of one detector module are connected in parallel and share the current provided by the source. Right: the Shunt-LDO circuitry inside the ROC regulates the voltage needed by the analog and digital parts ($\sim$ 1.2 V) ensuring the flow of the current provided by the source. Separate SLDO, working in parallel, power the digital and the analog domains of the chip.

The Phase-2 tracker power budget also demands an effective cooling system to remove the heat generated inside the tracker volume. An innovative cooling system, based on two-phase CO_2 coolant and operated by five 50 kW cooling plants (-35 °C set point), allows to operate the silicon below -20 °C. The reduced dimensions of the pipes used by this cooling system help in maintaining low the material budget inside the tracking volume.

5. Summary

The upgraded CMS tracker is going to be a radiation-hard and highly segmented detector designed to operate in the harsh HL-LHC environment and to provide excellent tracking performance,

extended η coverage, luminosity measurement and L1 trigger primitives at 40 MHz. The performance is resting on top of innovative modular, lightweight design choices and new technologies: new rad-hard ASICs and optical links, rad-hard thin silicon sensors, innovative powering schemes and CO_2 cooling. Figure 6 shows the expected performance enhancement according to simulation studies. The mechanical layout and the integration studies are in advanced status: the assembly of

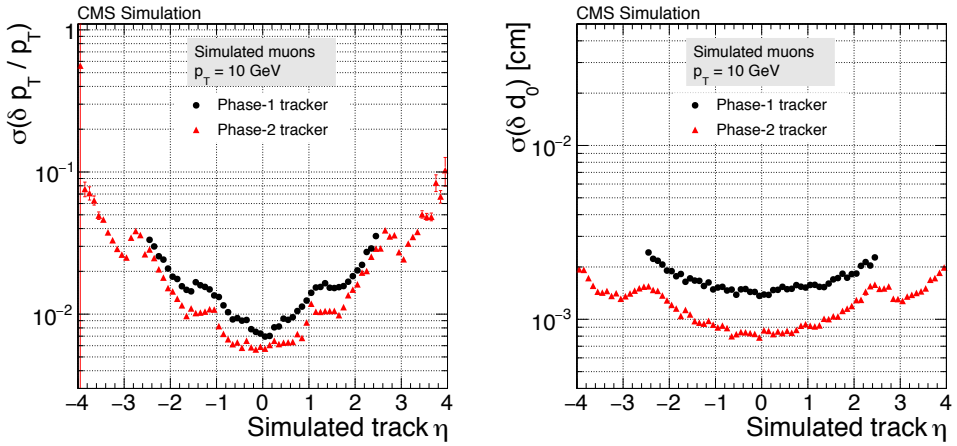

Figure 6: Track parameter resolution for the Phase-1 (black dots) and the Phase-2 (red triangles) tracker, from the simulation of single muons with a transverse momentum of 10 GeV. The p_{T} resolution (left) and the impact parameter resolution (right) show the improved performance of the Phase-2 detector [3].

the first module prototypes and the submissions of final ASIC prototypes are expected in 2020.

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