PROCEEDINGS OF SCIENCE

Test benches for the upgrade of the Pierre Auger Observatory electronics

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The Pierre Auger Observatory, the largest cosmic ray detector ever built, has been collecting scientific data since 2004. As part of the AugerPrime upgrade, the Observatory is currently undergoing a modification of the surface detector stations, which involves a replacement of their electronics with a faster and a more powerful system that provides channels for additional detectors as well as increased dynamic range and processing capability, higher sampling frequency, and improved timing, calibration and monitoring systems. The testing of the new electronics boards will be conducted in three stages: the production test performed at the manufacturer site, the climate tests including accelerated ageing executed in a laboratory and finally the full functionality tests effectuated before the deployment at the Observatory in Argentina. A description of the test benches and the testing procedures is given together with some examples of the performance of the prototype.

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1. Introduction

The Pierre Auger Observatory design features a large detection area collecting unprecedented event statistics, a combination of several detection techniques allowing one to lower the systematic uncertainties of the results obtained, and constitutes a continuous effort of more than 450 scientist from 17 countries. The amount of gathered scientific results largely surpasses the original expectations. The Surface detector (SD) array is formed by 1660 water-Cherenkov detectors (WCD) placed in a triangular grid with 1500 m spacing on the area of around 3000 km^2. The array is fully efficient above 3×10^{18} eV and continuously samples both the electromagnetic and muonic parts of the extensive air showers (EAS) with nearly 100 % duty cycle. The WCDs are overseen by 27 fluorescence telescopes located on the boundary of the array, observing the longitudinal profile of the electromagnetic component of the air shower. Fluorescence detector (FD) can only be operated during clear moonless nights. A thorough description of the Observatory is given in [1].

After fifteen years of operation the Observatory is being upgraded. The main scientific aspects motivating the upgrade are the following: lack of primary mass composition information at the highest energies, the observation of the composition getting heavier with higher energy hampering anisotropy searches, and the discrepancies between hadronic interaction models and the measured shower parameters. The upgrade, currently underway, aims at resolving these issues. Each WCD will be equipped with a 4 m^2 plastic scintillator mounted on the top (Surface Scintillator Detector or SSD). The two detectors will provide complementary information about the electromagnetic and muonic components of the shower. An additional Radio Detector (RD) will be mounted on top of each WCD for the observation of radio signal in 30 – 80 MHz band from inclined showers to add yet another measurement of the electromagnetic component. Adding a small, less sensitive PMT to the three already in place inside the WCDs will enlarge the dynamic range and permit one to study signals closer to the shower core. Finally, buried scintillators will accompany 61 SD stations to provide a pure muon signal on a small sample of showers (AMIGA - Auger Muons and Infill for the Ground Array). A more powerful, modernized electronics will allow one to interface the additional detectors as well as the current ones. Faster FADCs with higher resolution will resolve a finer temporal structure of the signals. A comprehensive description of the Observatory upgrade can be found in the Preliminary Design Report [2].

2. Upgraded Surface Detector electronics

To accommodate the baseline design detectors as well as the additional detectors of AugerPrime, the current Unified Board (UB) will be replaced by an Upgraded Unified Board (UUB), providing four additional channels. It has to fit into the same RF enclosure with only the front panel replaced and has to accept the existing PMT, GPS antenna and communications cables. The new UUB integrates data acquisition, analog signal processing, triggering, calibration and Slow-Control (SC) functionality on a single board. The new electronics design features more powerful FPGA (Xilinx Zynq-7020) together with 512 MB RAM, a 256 MB Flash memory, and faster ADCs (120 MHz instead of 40 MHz) with larger dynamic range (12 bits instead of 10 bits). New triggers are implemented using digital filtering, which permits one to reproduce the current trigger characteristics so that data taking can continue during the deployment period.

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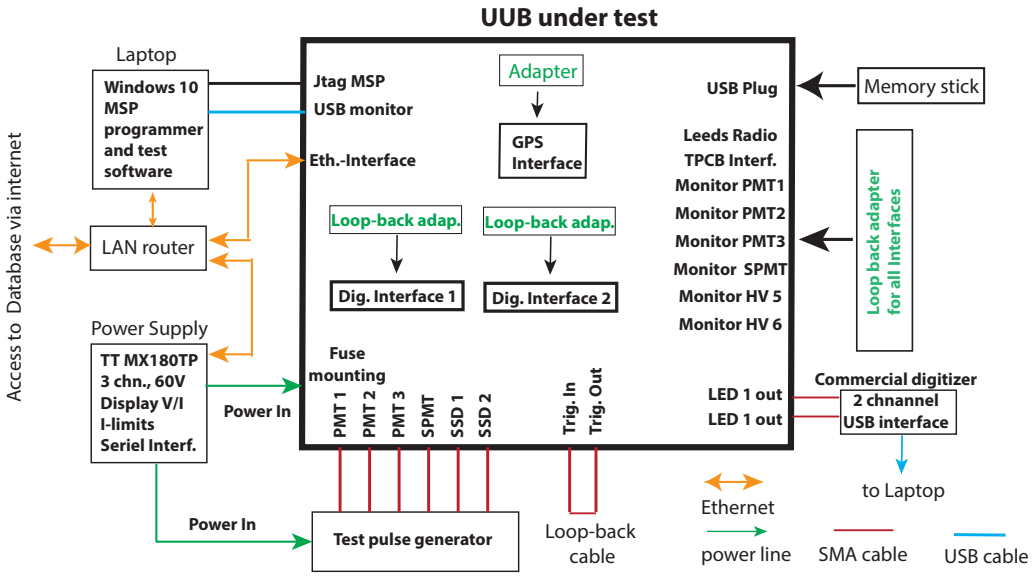

Figure 1: Scheme of the production test setup.

All analog inputs accept signals up to 2 V except the SSD channel, which accepts up to 8 V. Each PMT signal is split into two branches with different amplification gain, high gain (HG) and low gain (LG), and passed through an anti-aliasing filter with the cut-off frequency of 60 MHz. Therefore the HG/LG ratio is designed to be 32 (or 128 for the ratio of the SSD channels) and is set purely by resistor values in the analog front-end. The SlowControl part of the UUB is responsible for controlling the power supplies and PMT voltages, watchdog and reset functions. In addition, the SC monitors currents, voltages, temperature and humidity. It is implemented by micro-controller MSP430. Detailed description of the new SD electronics can be found in [3].

3. Production test

The purpose of the Production test is to verify that all functional blocks of the UUB were assembled correctly and to program the MSP430. All tested UUB interfaces are connected: the power supply connector to a programmable power supply (TT MX180TP), the SMA front-end inputs to a test pulse generator, the GPS interface to an adapter, both digital interfaces to loop-back adapters, the D-Sub type connectors for controlling and monitoring of PMT high-voltages to loop-back adapters. Further, the LED outputs are connected to a commercial digitizer, the Ethernet interface to a LAN router, the SMA connectors trigger out to the trigger in, the USB host connector to a memory stick, the USB device connector to the test computer, and MSP JTAG connector to a JTAG programmer.

The test proceeds in the following eight steps: 1) the UUB supply voltage is varied over the allowed range ($19\,\mathrm{V} < U_{\mathrm{in}} < 32\,\mathrm{V}$) and the system checks that UUB's voltage limiter switches the UUB off in case of under or over-voltage; 2) SlowControl MSP is programmed via JTAG, the UUB is powered off/on - the MSP is expected to start and the UUB to boot PetaLinux on Zynq cores; 3) UUB internal voltages and currents drawn are read out of SC and compared with the prescribed values; 4) electrical connections to the GPS interface, to the radio connector and the digital interfaces

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are verified by generation of appropriate signals and read out via loop-back adapters; 5) a ramp signal is generated at both LED outputs and acquired by a two-channel commercial USB digitizer to verify the signal shape; 6) PMT-like signals are sent to the six SMA front-end inputs by a custom made test pulse generator, recorded by the UUB, transferred to the test system (via Ethernet) and analyzed. Parameters as baseline, RMS noise, pulse amplitude are determined and verified to be within prescribed margins; 7) access the memory stick in the UUB host connector is verified; 8) finally, a reset command is issued via the radio interface to verify that the UUB restarts. All tests are evaluated and the test results are uploaded into a dedicated database.

4. Environmental stress screening

Environmental stress screening (ESS) is performed to characterize the behaviour of the new electronics under changing environmental condition and to provoke early failures. Climate tests are conducted in three stages: the pre-test, burn-in and temperature cycling. The purpose of the pre-test, which is performed on individual boards, is to diversify the MAC addresses, to measure the noise of the analog chain with open connectors and to acquire a thermal image of the powered UUB in order to discover thermal irregularities. After the pre-test the burn-in and thermal cycling is performed with a batch of ten boards at the same time. The scheme of the test bench for temperature cycling is shown in Fig. 2. The test bench consists of a climate chamber (MKFT 115, Binder), test function generator (AFG3252C, Tektronix), a power supply (HMP 4040, Rohde&Schwarz) and custom devices: a signal distribution board, a power control board and a trigger fan-out. The temperature inside the chamber is monitored by the chamber itself as well as by two sensors BME280 (Bosch).

The signal distribution board is designed to fan-out the signal from the function generator to the 60 channels on ten UUBs (50 Ω impedance). It operates in three modes: a) the attenuated mode, where the input signal is attenuated by a factor 32 (for testing HG UUB channels), b) the frequency mode, where the input signal is propagated to all 60 outputs with unmodified amplitude (bandwidth 70 MHz, maximum output amplitude 2 V_{pp}), and c) the amplified mode, where the input signal is propagated to 50 UUB inputs (5 per UUB) with the same amplitude and amplified by a factor of 4 to the 10 SSD inputs (bandwidth 10 MHz, maximum output amplitude 8 V_{pp}). The power control board monitors the current drawn by individual UUBs and allows to switch individual UUBs off in case of a failure. The trigger board distributes the trigger signal to the UUBs with a programmable delay.

4.1 Temperature cycling and burn-in

During the temperature cycling 10 UUBs are placed inside the climate chamber at a minimum distance 5 cm from each other. During the burn-in process the temperature in the chamber will change rapidly in the range $-20\,^{\circ}$C and up to $70\,^{\circ}$C to provide a maximum thermal stress. The temperature range is slightly larger than the range the UUBs have to face in the pampas. Only an Ethernet connection for read out and control, a power supply and an external trigger will be attached to allow monitoring of the noise, ADC bits functioning and SC values.

The burn-in is followed by 10 cycles with intermediate measurement points. Additional 6 SMA connectors have to be mounted on each UUB in order to provide analog test signals. The

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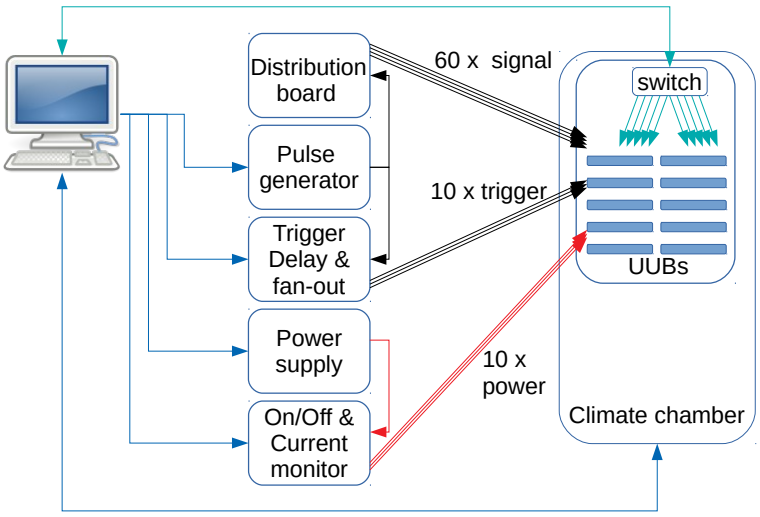

Figure 2: Scheme of the experimental setup for climate tests.

cycling starts at 20°C going down to $-20\,^{\circ}\mathrm{C}$ and up to $70\,^{\circ}\mathrm{C}$ - the same range as the burn-in but this time with a temperature change of $\sim 3\,^{\circ}\mathrm{C/min}$). Every 20 – 25 °C a 1-minute interval for measurements and readout follows after 5 minutes of temperature stabilization (14 + 1 minute at the extreme temperatures). Thus, the measurement points are: 20, 0, -20, 0, 20, 45, 70 degrees Celsius. In the last cycle a power ON/OFF test is performed at extreme temperatures. During the whole cycling process, the current drawn by each UUB, temperature readings from the chamber, BME280 sensor, Zynq as well as SC values are monitored. In case of a critical quantity outside of limits the operator is notified.

The duration of both testing parts is approximately equal ($\sim 21\,\mathrm{h}$). Thus, 20 UUBs will be tested in 48 hours with sufficient time allowed for manipulation and maintenance.

4.2 Measurement point - performed tests

- **Noise test:** The pedestal and noise RMS for each channel is derived from the whole ADC trace, when no input signal is present.
- **Linearity test:** The test pulse consists of five half-sine pulses connected with a baseline. The test pulse is issued with twelve amplitudes covering the whole dynamic range of the ADCs. The recorded trace is fitted by a model function and its amplitude is calculated. The gain is derived from a linear regression of input and output amplitudes.
- **Frequency test:** The test pulse is a burst of sine waves, 22 µs in length. The external trigger is adjusted such, that the recorded sine wave spans the full UUB acquisition window (17 µs). Voltage amplitudes of $1.6\,\mathrm{V_{pp}}$ for LG and $50\,\mathrm{mV_{pp}}$ for HG channels are used at seven frequencies (10 MHz, 20 MHz, 30 MHz, 40 MHz, 50 MHz, 59 MHz and 70 MHz). The measured signal is fitted by a sum of a sine and a linear function. The cut-off frequency (i.e. 3 dB drop) is calculated from the fit parameters for each channel.

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- **Ramp test:** Analog inputs are disabled during this test and ADCs are switched to a mode, where they generate an internal ramp signal. Sequential ADC values are required to increase by one ADC count.

- **Hot/cold start:** In cycle 9 high temperature, the UUB power supply voltage will be gradually increased until all the UUBs shutdown. Then the voltage will be gradually decreased below 32.4 V – all UUBs are expected to restart. The point of shutdown and startup of each UUB will be recorded. Next, the temperature cycle will continue down to $-20\,^{\circ}$C, where an analogical procedure will be conducted. The required low voltage limit there is 19.1 V.

4.3 Automation of data acquisition and storage

The test run is controlled by a computer with devices connected via USB (the climate chamber, the function generator, the power supply, the power control, the trigger delay, the environmental sensors), UUBs under test are connected via a Gigabit Ethernet router. The controlling software is implemented in Python and functions interfacing particular devices are run in separate threads in order to avoid I/O limitations. To read *slow* quantities out of the UUB an embedded HTTP server is used and commands are send to the UUB via a dedicated HTTP request. The UUB FPGA features four buffers for ADC traces. As the test function parameters (the function type, amplitude, frequency, the distribution board mode) vary, it is necessary to match an acquired ADC trace with these parameters unambiguously. For this purpose, a dedicated C-based code running on the UUB periodically checks if a new ADC trace is available, reads the ADC trace out, splits raw data into parts and sends them as a bunch of UDP packets with a simple header to the control PC. On the control PC side, a dedicated Python thread listens for these UDP packets, assembles them, converts them into a NumPy array, bundles them with the test function parameters and passes them to a data processing thread. If all UDP packets for a particular ADC trace are not received within a predefined timeout interval, the ADC trace is discarded, thus allowing a reliable recording of hundreds of ADC traces per second. Measured data together with monitoring values are stored in the database.

5. SD station simulator

The SD station simulator is designed as a standalone portable test system, which can be used for the final functional test reproducible later in other laboratories. Functional blocks of the system are depicted in Fig. 3. The system is governed by an industrial single-board computer (SBC) running Scientific Linux, a LabVIEW based graphical user interface, test control software, and a ROOT/C++ data analysis software for evaluation of recorded pulses. The SBC communicates via USB with other components: a custom developed DAC card featuring 6 analog outputs, a power card providing all internal supply voltages as well as power supply for UUB, a Labjack U12 DAQ card, and an extension amplifier card.

The DAQ card serves for monitoring voltages generated by the the UUB to set the PMT high voltage (HV). For testing of the UUB SSD channels featuring an -8 V range, an extension amplifier card providing the required range with $50\,\Omega$ output impedance is integrated into the system. A Landau-shape pulse is generated by a custom made DAC card based on Zynq 7020 (the same

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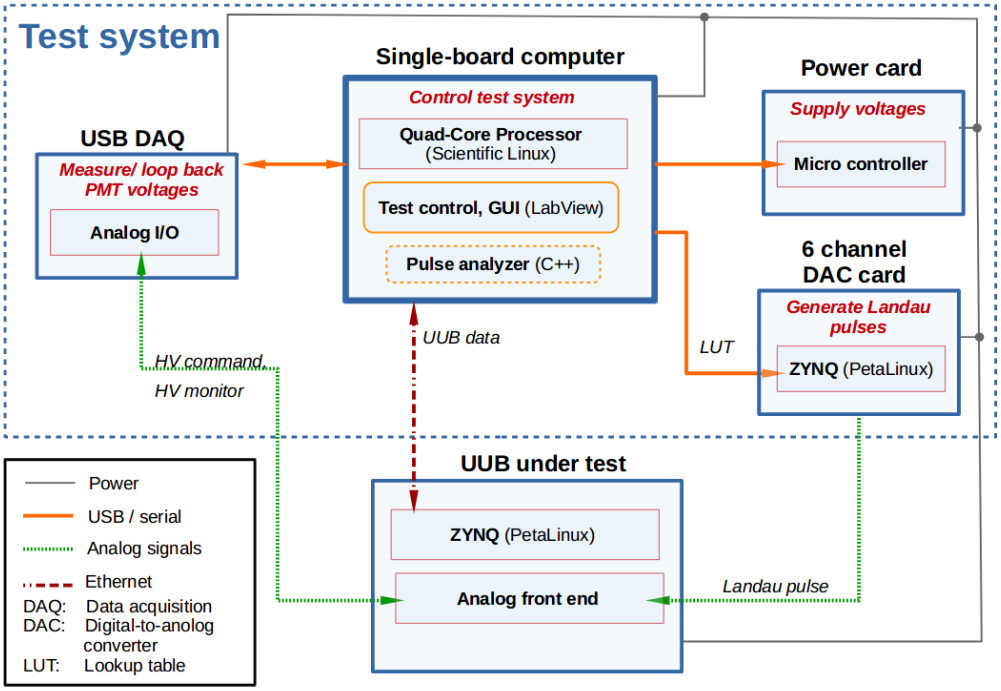

Figure 3: Block scheme of the portable test system setup.

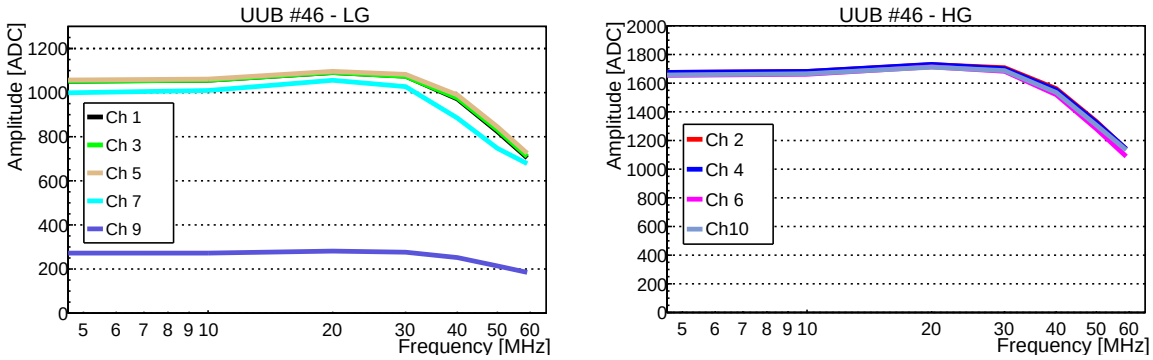

Figure 4: Performance of the UUB V1 prototype under frequency test.

as used in UUB) and three dual-channel 12-bit digital-to-analog converters (DAC) with 500 MSPS rate.

The system performs two tests: *Single pulse test* (SPT) and *PMT voltage test* (PVT). In the *Single pulse test* the system generates a Landau pulse shape (of two amplitudes: 50 mV and 800 mV; and of two FWHM 40 ns and 200 ns) and sends it to analog inputs of the UUB. The pulses are sampled and the ADC traces analyzed. 100 pulses are issued per each configuration, out of which mean values of measured amplitude, FWHM, pulse rising and falling edges, and pedestal position and noise are calculated. In the *PMT voltage test* the system instructs the SC to set the control voltage for the PMT HV (range 0 – 2.5 V) via DAC and outputs it on a dedicated pin on the D-Sub interface. The system reads out this voltage via DAQ card and compares it with the expected value.

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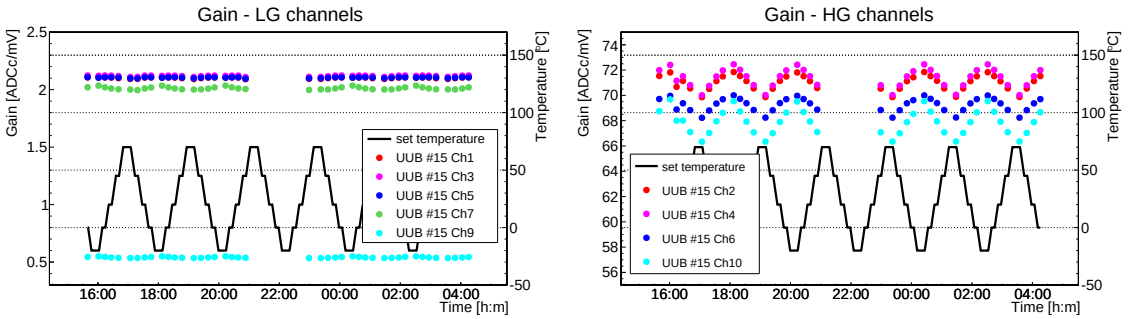

Figure 5: Temperature dependence of the gain of the analog chain.

6. Performance of the prototype UUB

Three UUBprototype versions have been developed and tested in the preparatory period. Two examples of the version 1 UUB performance are shown in Fig. 4 and 5. The scan in frequency described in Section 4.2 was performed using a sine wave with amplitude 500 mV for LG and 25 mV for HG channels. The results presented in Fig. 4 show a good performance of the anti-aliasing filter. The gain of each channel is derived from the linearity test and plotted as a function of temperature in Fig. 5. The temperature dependence of the gains observed in version 1 is expected to decrease in the final version of the UUB. However, the calibration in the field is done every minute so any remaining fluctuation will be taken into account. Further examples of the performance of the new electronics are presented in [4].

7. Conclusions

Three types of test benches were prepared to cover essential tests and characterization of the new surface detector electronics before being transported to the Pierre Auger Observatory site - the production test bench, the ESS test bench and a portable test system.

Acknowledgments

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