

# FELIX: the New Detector Readout System for the ATLAS Experiment

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Starting during the upcoming major LHC shutdown (2019-2021), the ATLAS experiment at CERN will move to the Front-End Link eXchange (FELIX) system as the interface between the data acquisition system and the trigger and detector front-end electronics. FELIX will function as a router between custom serial links and a commodity switch network, which will use industry standard technologies to communicate with data collection and processing components. This paper describes the FELIX system design as well as the results of the ongoing development program.

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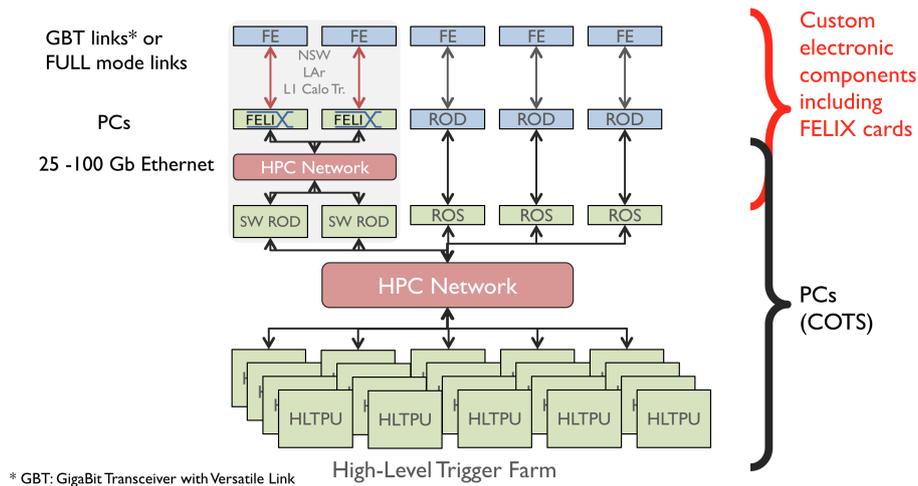
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## 1. Introduction

After the upcoming LHC shutdown (2019-2020), the ATLAS experiment [1] will be required to operate in a significantly harsher collision environment. The LHC will deliver luminosities up to three times the original design value, with a commensurate increase in the number of interactions per bunch crossing. To maintain physics performance in this new regime, the ATLAS experiment will undergo a series of upgrades during the shutdown. Among the upgraded components there will be the Trigger and Data Acquisition (TDAQ) system, which in the new environment will have to process significantly more complex events while maintaining stable the selection performance [2]. At the same time, the TDAQ system will have to interface with new on-detector readout technologies for the new Muon Small Wheel detector, the upgrade of the Liquid Argon (LAr) Calorimeter and Calorimeter Trigger [3, 4]. In total, the new systems will require approximately 2000 new optical links to be read out by the TDAQ system. The upgraded ATLAS systems will make use of newer readout link technologies. To connect the new systems, and handle the significantly increased data volumes in a detector agnostic and easily scalable way, a new readout architecture named the Front-End Link eXchange (FELIX) is under development [5]. The FELIX system will be installed in 2019 and will operate alongside with existing readout system, as drawn in Figure 1.

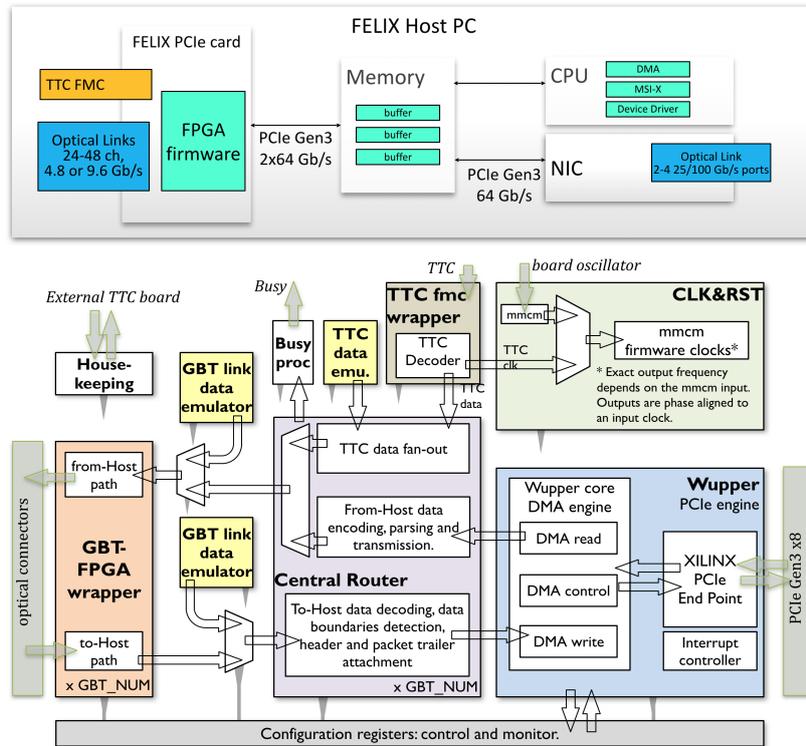


**Figure 1:** The ATLAS readout scheme planned for data taking between years 2021 to 2032. The FELIX system will be used alongside the existing readout setup.

## 2. The FELIX system

FELIX receives and identifies different information streams on its incoming optical links and routes packets to client processing applications via a commercial switched network. In the opposite direction, FELIX receives packets from the network and forwards them to specific on-detector modules. FELIX also handles input from the Timing, Trigger and Control (TTC) system to recover the LHC clock and forward synchronous trigger information to on-detector electronics over low-and-fixed-latency GBT links [6]. FELIX supports multiple different data encoding formats, including 8b/10b and HDLC, to satisfy the requirements both of primary dataflow and experimental slow control. The final FELIX system is implemented using third generation PCI express with

16 lanes providing a total bandwidth of 128Gb/s toward the host PC memory. The PC itself has to be connected to a High-Performance Network (HPN) as shown in Figure 2 top side.



**Figure 2:** Top: The FELIX system is implemented on a PCI express card and hosted in a PC. Bottom: The FELIX firmware design for GBT mode.

## 2.1 FELIX hardware and firmware

The most recent implementation of FELIX, named FLX-712, makes use of a custom built PCIe board with a Xilinx Kintex UltraScale FPGA, and 48 bidirectional optical interfaces in the form of eight Mini-POD transceivers (max. link speed 14 Gb/s) [8]. TTC decoding circuitry is hosted on a custom mezzanine board to enable future upgrades of the TTC system to be supported with minimal hardware changes. The optical links, PCIe interface, and TTC decoding circuits have been verified to function well in all prototypes [7].

The firmware provides support for two modes of operation: the so called GBT and FULL modes. The former uses the the radiation-hard Giga Bit Transceiver (GBT) protocol, running at 5 Gb/s and the latter, the high bandwidth FULL mode ‘FPGA-to-FPGA’ protocol, running at 10 Gb/s. The GBT links provide aggregation for up to 42 slower serial electrical links, making them critical for data collection from the front-end ASICs within the new systems. The information received from either protocol, together with the TTC information, is collected in the central router which uses the always running Direct Memory Access (DMA) engine to transfer the received data blocks into a contiguous memory area of the host PC, using it as a circular buffer. As the DMA operation runs continuously, it eliminates DMA setup overheads and achieves a high throughput: 12 GB/s for the FLX-712 card. GBT links can also be used for the propagation of control and configuration

data together with TTC information back to the front-end electronics. The FELIX firmware design for the GBT mode is presented in Figure 2 bottom side.

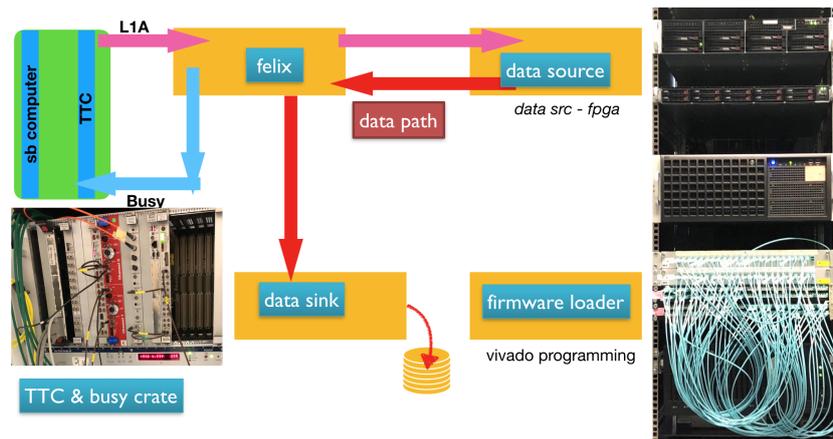
## 2.2 FELIX software

The FELIX software is organized with a multilayered approach. The available FELIX hardware is accessed through the in-house developed device drivers using the functions provided by the FELIX Application Programming Interface (API). There are a number of low-level tools using the FELIX API made available for user tests or hardware configuration. The main software program which will be used during data taking is the FELIX core application. It collects the data from the circular buffer and forwards them to the HPN using a home-grown network access library known as NetIO. Data can be served to multiple subscribed clients, such as the Detector Control Systems (DCS), Software Read Out Drivers or other custom clients. The whole software project is kept organized using the concurrent version control system GIT and additions from various developers are incorporated into the main stream using continuous integration tool GIT-CI.

The Felix core application provides minimal monitoring (for test stands) of the internal buffers, queue sizes and various transfer rates via a web based service. During ATLAS data taking, this monitoring service is to be replaced by a dedicated network client. The FELIX system also supports dynamic configuration of E-link properties on GBT links.

## 2.3 System Integration and Tests

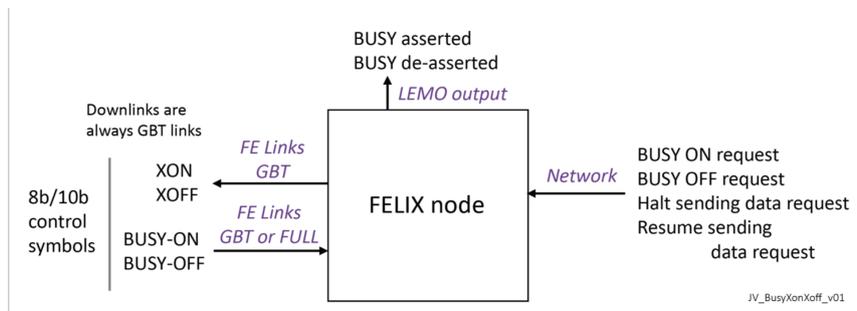
A validation test setup at CERN allows system integration and testing of major FELIX functionality and performance. As seen in Figure 3, a VMEbus crate provides trigger information to the FELIX system which forwards the L1 accepts to the FPGA based data source emulators triggering them to send simulated data packets. The received and concentrated data are forwarded to another PC acting as a data sink over a HPN. This setup realistically emulates the receipt of trigger information from the TTC system and the interaction of FELIX with detector front-ends.



**Figure 3:** The FELIX integration and test setup.

A recently implemented critical component is the busy mechanism as shown in Figure 4 . In normal operation using the FULL mode, XON and XOFF signals are used to throttle the transmission of data from the front-end to FELIX to prevent buffer overflow. For GBT mode, a BUSY will

have to be asserted directly. The BUSY assertion expresses an emergency situation with impending buffer overflow, resulting in all ATLAS data taking being paused, and is not intended for normal flow control. The BUSY signal will be de-asserted once there is no BUSY condition satisfied. BUSY assertion has been successfully tested in the validation test setup.



**Figure 4:** The FELIX Busy mechanism summary.

The validation test setup is used for automated tests for different hardware, firmware and software versions. Every night, a user defined number of firmware candidates are loaded automatically into the appropriate FELIX hardware to execute a set of predefined operations and compare their output to reference values. The results of these tests are kept in an easily accessible format and served via a web interface. Integration of the FELIX software tests into the same nightly scheme is planned to validate both firmware and software release candidates.

### 3. Outlook

Regular releases of the FELIX firmware and software are distributed to sub-detector front-end developers. Integration and testing with the final prototype of the complete FELIX firmware and software infrastructure is an ongoing process aiming to increase overall system reliability. The results of these tests show that the packet processing performance of the design satisfies ATLAS readout requirements for 2021 for both GBT and FULL mode operations. The procurement of the final system components is currently ongoing. The installation of the first FELIX systems in ATLAS is planned for 2019.

### References

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