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The VMM front-end integration in the Scalable Readout System: On the way to a next generation readout system for generic detector R&D and experiment instrumentation

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The Scalable Readout System (SRS) of the RD51 collaboration with the APV25 ASIC is driving R&D for gaseous detectors. Discontinuation of APV25 and demands on flexibility concerning e.g. detector capacitance and readout rate induced a replacement of the ASIC, for which the collaboration has chosen the VMM chip of the ATLAS New Small Wheel upgrade. A prototype SRS VMM system was operated with small GEM detectors at test beams and hardware components are finalised. More than twelve groups signed as primary system users. We present the readout chain and current status of the implementation of the VMM in SRS, applications and further developments.

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1. Introduction

Within the RD51 Collaboration [1], groups from about 90 institutes are working on R&D and the application of Micro-Pattern Gaseous Detectors (MPGDs) [2]. This community has developed common readout electronics, configurable for different types of detectors, scalable from a table-top R&D system to large experiments and generic to implement different front-end Application Specific Integrated Circuits (ASICs): The Scalable Readout System (SRS) [3]. The first ASIC implemented when the system launched in 2009 was the APV25 [4]. Still today, this realisation of SRS is the one most frequently used and backbone for the readout of MPGDs, even though other ASICs have been implemented since. Several R&D projects and experiments have been carried out with this system. However, the production of APV25 ASICs has been discontinued and the stock of chips is almost exhausted. Therefore, the RD51 collaboration has decided to implement the VMM ASIC [5] as primary frontend choice for the next generation of SRS. This chip was developed by Brookhaven National Laboratory for the ATLAS New Small Wheel upgrade [6] and is outfitted with flexible configuration parameters and hence, fits the SRS philosophy.

2. SRS with the VMM front-end

In the framework of the Horizon2020 projects BrightnESS and AIDA2020, the VMM ASIC was implemented in SRS [7, 8, 9]. This system is called *SRS VMM* in the following. The architecture follows the general SRS design, as shown in Fig. 1. From the detector side, the readout chain starts with the *hybrid*. This component is a Printed Circuit Board (PCB) with two VMM ASICs to read out 128 channels of charge collecting structures in the detector through a protection circuit against high charge from sparks. Data from the two VMMs is then combined in a Spartan-6 Field Programmable Gate Array (FPGA) on the hybrid, which also forwards control sequences to the ASICs. The hybrid is connected to an *adapter card* via an HDMI cable, which can be used for powering. A custom protocol for Data, Trigger, Clock and Control (DTCC) [10] is operated on the link. The adapter card interfaces to the general SRS components used in every implementation: the Front-End Concentrator (FEC) card as back-end and in addition for large systems either a Scalable Readout Unit (SRU) or a combination of a standard Ethernet Switch and a Clock Trigger Generator Fanout (CTGF) card. The readout chain ends at the computer running slow control and data acquisition software. The colour code in Fig. 1 resembles commercial components (blue), SRS general hardware (green) and ASIC specific hardware (orange). To implement a new ASIC, the hybrid, as well as the firmware of an FPGA on the FEC need to be developed. For ASICs with fundamental different requirements (data type, analogue/digital output, bandwidth), a redesign of the adapter card might be required as well.

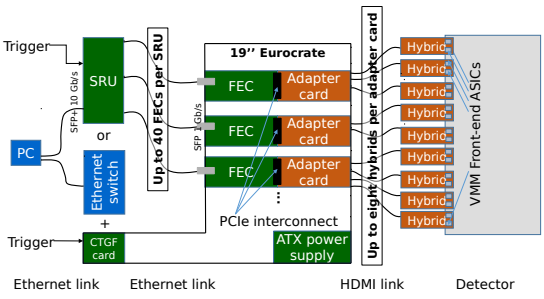

Figure 1: Architecture of SRS VMM following the general SRS design. The colour code resembles commercial components (blue), SRS general hardware (green) and ASIC specific hardware (orange).

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3. Status of VMM implementation

The design of the implementation of the VMM ASIC in the SRS has been outlined in [7] in detail. In this section, we report on the current status of the system. Within the last three years and in parallel to the design of the VMM ASIC, the readout system has been developed with several iterations of hardware and continuous firmware and software improvements.

3.1 Hardware

Fig. 2 shows different versions of the hybrid (left) and adapter card (right). For the hybrids, the final version is available and a few prototypes were tested successfully. Compared to the previous version, it features the final VMM3a chip, two additional I2C Analogue Digital Converters (ADCs) to measure voltage levels on the monitoring outputs of the VMM as the internal temperature, the baseline or threshold of a configurable channel. The connector to the detector has been replaced to the new Hirose standard. In the future, the I2C ADCs will be used to scan the threshold and pedestal of all channels, perform automated response equalisations and to qualify a cooling system.

For the adapter card, the final version is currently being designed and will implement an improved powering scheme to supply all eight hybrids. The most significant change is a preparation for a *master/slave* mode, in which two hybrids can be connected to one HDMI input channel of the adapter card. For this scheme, an additional component, called *power box*, will be necessary between adapter card and hybrid. It will serve as a splitter and provide power for up to 16 hybrids, for which the supply from the adapter card is insufficient.

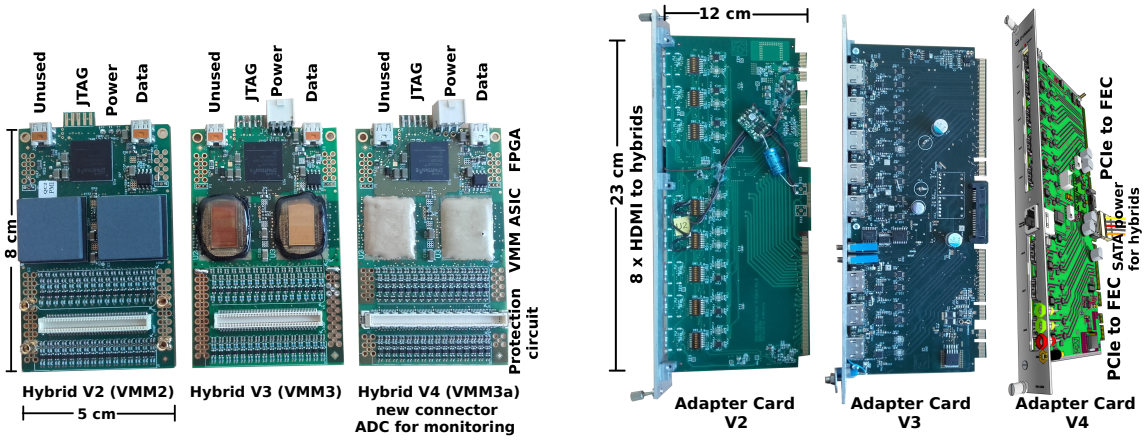

Figure 2: Hardware components developed for the implementation of the VMM ASIC in the SRS. The different iteration versions for the hybrid (left) and adapter card (right) are shown. The final adapter card V4 is currently being designed.

3.2 Firmware

Basic functionality is implemented in the firmware and it has been operated since about two years to transfer data and control VMMs at test beams and in the laboratory. Still, it is continuously improved. The readout speed of data from VMM to Spartan-6 FPGA on the hybrid was increased

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from 40 Mbit/s to 640 Mbit/s, where 800 Mbit/s is the limit. Further investigations are necessary to reach that limit, as bit flips were observed in the data stream or its capture in the FPGA.

The way data is treated in the FEC was re-evaluated and modified, such that is is capable to stream all data from the hybrids to the computer in the most efficient way. Within the firmware, the throughput, even in a master/slave scheme is sufficient to transfer data at the maximum rate that can be achieved by the VMMs until the Gigabit Ethernet part of the firmware, where the physical link remains the bottle neck. In an experiment with low or non-continuous rate, this must not be a problem. In order to store large amounts of data that could be acquired during e.g. a collision or particle spill, access and control to the DDR3 memory on the FEC has been implemented into the firmware.

3.3 Software

Several software tools have been developed with the Data Management and Software Center (DMSC) of the European Spallation Source ERIC (ESS), as online monitoring and data acquisition. Together with our slow control software, those independent tools will in the future be combined into a new VMM DAQ, for which a working group has been set up.

4. Test beam

Besides tests at gaseous detectors as GEM [11] or Micromegas [12] in the laboratory, the electronics was also tested in a pion or muon beam of the SPS at CERN with a triple GEM detector. Milestones were the first tests with VMM3 hybrids in August 2017, the full instrumentation of a 10 cm $\times$ 10 cm detector in October 2018, see Fig. 3 and the first VMM3a hybrid in August 2018. Those tests were in particular interesting to test different parameters of the VMM ASIC, the firmware throughput and develop data analysis software. Results are still mitigated by unequal responses to the same charge between the channels, as a calibration procedure is not yet implemented.

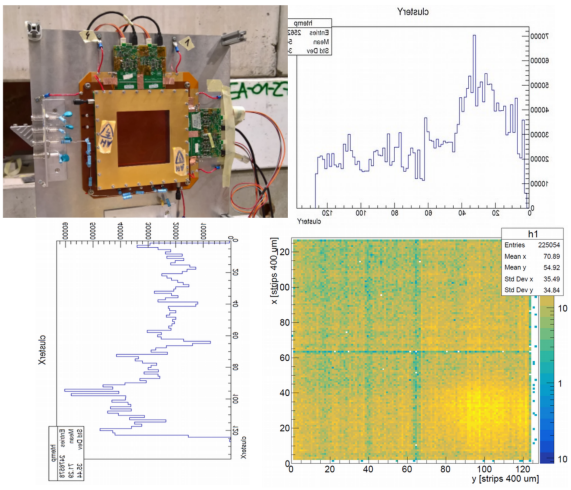

Figure 3: Beam test of a triple GEM detector with SRS VMM readout at the CERN SPS. Experimental setup (top left), x and y projections of the beam profile (top right and bottom left) and reconstructed beam profile (bottom right).

5. Conclusion and applications

The VMM ASIC has been implemented in the SRS and the project is about to be finished. Currently, hardware components are finalised, firmware is improved and a comprehensive data acquisition developed based on different already existing tools. Even though the system is in a prototype state, it is already requested by more than twelve different groups from High-Energy Physics (HEP) but also other fields to apply it as readout for R&D projects and upcoming experiments.

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6. Outlook

To handle enormous amounts of data in a streaming readout, which does not internally reduce data and forwards all information to a computer cluster for further treatment, the current FEC is limited by its Gigabit Ethernet link. For the VMM, this is already the bottle neck in the readout chain. In the future, ASICs will output even larger amounts of data, such that a revision of the FEC should be considered. To start his process, state-of-the-art readout systems of HEP and neighbouring fields should be evaluated in detail. Current trends to move away from pure FPGA suggest to implement a System on Chip (SoC), combining real-time processing with computing power of a CPU, and an output bandwidth in the regime of 100 Gbit/s.

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