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A Capacitor DAC for Charge Redistribution Analog to Digital Converter with Successive Approximation

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The recent analog to digital converters, with the successive approximation (SAR ADC), are widely used for their high speed, low power operation and accuracy. SAR ADC demands precise internal digital to analog converter (DAC). To save power, the DAC is mainly implemented using capacitors (CDAC). Its precision depends mostly on layout implementation which must minimize the various parasitic effects. This paper presents two new layout design approaches of CDAC for SAR ADC used in a pixel detector implemented in 180 nm SOI technology. The various types, topology, size of the capacitors, power consumption, layout area, speed, and any nonlinearities are discussed. First is a new layout design of the 10-bit split capacitor DAC with Metal-Insulator-Metal capacitors, and, the second, is a 8-bit binary-weighted DAC with Metal-Oxide-Metal capacitors. The new layout of the metal-oxide-metal capacitor topology provides better accuracy of the DAC. The layout styles for each of CDAC, with low parasitic capacitances, are shown. The post layout simulations confirm that both capacitor arrays have an integral, differential nonlinearity, less than one least significant bit without a calibration scheme.

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1. Introduction

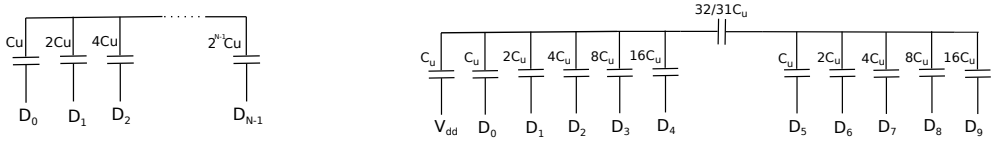
A switched capacitor, digital to analog converters (CDAC), is used for its low power, fast and accurate performance. Most of the papers are dedicated to the SAR ADC design [1], [2]. However, a CDAC design oriented paper is hard to find. Therefore this paper provides us with two new layout styles as a guideline on how to design CDAC for SAR ADC taking into consideration size and type of capacitor, power consumption, layout area, speed and nonlinearities.

The CDAC for SAR ADC is mostly designed with respect to integral and differential nonlinearity (INL, DNL) under 1/2 of the least significant bit (LSB). An important parameter of CDAC is also the gain error (slope of transfer function). The INL, DNL and gain error directly affect the performance of the SAR ADC. The main sources of these errors in the CDAC are the parasitic capacitances. The INL, DNL and gain errors can be alleviated by increasing the capacitance of the unit capacitor in the CDAC array and also with a proper layout technique. On the other hand, increasing the capacitance of the unit capacitor size increases power consumption and decreases the speed of SAR ADC. The type of the unit capacitor is also crucial. Generally, MOM and MIM capacitors are used for the CDAC design. Another approach for the alleviation of CDAC nonlinearities is to use a calibration scheme. The two main drawbacks in calibrating CDAC are the higher circuit complexity, resulting in higher power consumption and the calibrating circuits lowering the SAR ADC speed.

This paper shows two ways in which to implement 10-bit CDAC and 8-bit CDAC for column SAR ADC without a calibration scheme. The second section shows the differences between split and binary-weighted CDAC architectures. The third section discusses the capacitor types. The fourth section demonstrates the layout realization and discusses INL, DNL versus unit capacitor size. The fifth section shows our simulation results with the last section concluding this paper. The integral nonlinearity is computed according to the following reference [3].

2. Binary-weighted vs Split CDAC

This section shows the two realizations of the CDAC at schematic level. A binary-weighted capacitor array schematic is shown in Fig. 1a. The binary-weighted CDAC has better nonlinearities, but, on the other hand, it occupies a large layout area. The overall capacitance (sum capacitances of the all unit capacitors) of the binary-weighted type can reach a high value since the capacitance for each bit doubles the size. It results in higher power consumption in comparison with the split CDAC.



(a) Binary-wighted CDAC schematic

(b) 10-bit split CDAC schematic

Figure 1: CDAC architectures

The 10-bit split CDAC schematic is shown in Fig. 1b. The 10-bit split architecture needs only 64 unit capacitors. Also, the split design can save more power, because the overall CDAC capaci-

tance can be less. However, the split architecture suffers from higher nonlinearities. Moreover, a split capacitor has to have a proper value. The unit capacitor in the split design has to have a larger size to alleviate nonlinearities which decrease speed.

3. Unit Capacitor

In the CDAC design, Metal-Insulator-Metal (MIM) or Metal-Oxide-Metal (MOM) capacitors are frequently used. The MIM capacitor has a high capacitance density per area, and models of the Monte Carlo simulation are often available, but suffer from higher parasitic capacitances. The advantage of the MOM capacitor is the "cage" structure published by Liu at al. [1]. The proposed new cage capacitor is shown in Fig. 2. The metal 1 up to metal 4 and vias between them form the box (cage) which is one terminal V+ of the capacitor and the second terminal V- is formed by metal 2 and metal 3. The proposed capacitor has the nominal capacitance of 4.5 fF and size 4.3×4.3 µm^2. Note that the second terminal V- is connectable from all four sides. It simplifies the layout design. The electrical field of the cage capacitor is completely enclosed in the box, and therefore the parasitic capacitances at V- terminal are low. The V- terminals of all capacitors have to be connected together at the comparator input. Then the parasitic capacitances at the V+ terminal do not affect the performance of CDAC.

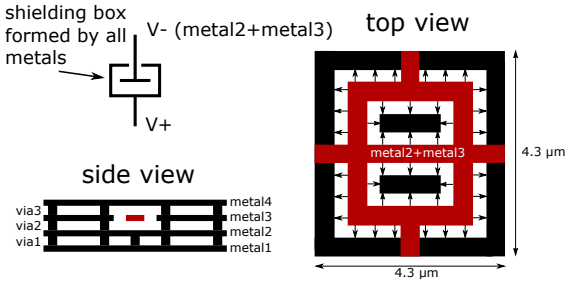
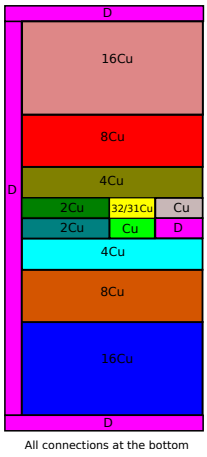


Figure 2: The proposed new topology of MOM capacitor

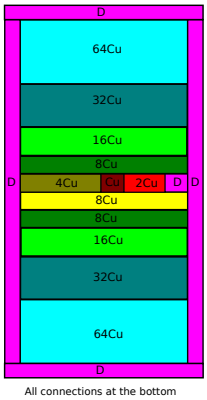
4. CDAC Layout Design

In this section, two examples of the CDAC layout design are shown. The first design is the 10-bit split CDAC shown in Fig. 3a corresponding to the schematic in Fig. 1b. The second layout design is the 8-bit binary-weighted CDAC in Fig. 3b with customized MOM capacitors in Fig. 2. Each of color in Fig. 3 stand for a particular bit. The D symbol stands for dummy devices.

The split CDAC contains MIM capacitors with a unit capacitance of 106 fF. The unit capacitance has to be high enough to keep INL and DNL low. Unfortunately, the high unit capacitor value deteriorates the speed of SAR ADC. The overall capacitance of the split capacitor array is 6.678 pF. In the array 63 MIM's are used for DAC operation and 1 dummy MIM is used to keep symmetry. The thin dummy MIM's surrounding the CDAC limits etching problems. At the right side, dummies are not needed because there is another CDAC for the next SAR ADC. The split capacitor is placed in the middle. No common centroid technique is used. This split CDAC was used in a radiation imaging detector and SAR ADC works correctly. The size of the split CDAC



(a) 10-bit split CDAC layout



(b) 8-bit binary-weighted CDAC layout

Figure 3: Proposed CDAC layouts for a pixel detector

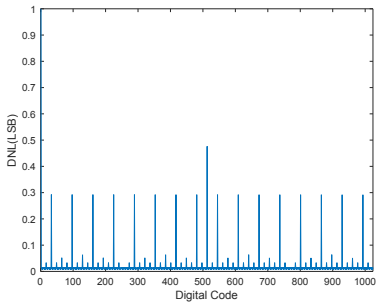
layout is 236×57.5 μm^2. The second CDAC layout design is in Fig. 3b is 8-bit DAC. It contains 256 customized MOM capacitors depicted in Fig. 2. The dimensions of this array are 196×57.5 μm^2. A SAR ADC with this binary-weighted array reaches a speed of up to 10 million samples per second (Msps). The overall capacitance of all capacitors is 1.174 pF. This allows for low power operation. The most sensitive node to the parasitic capacitances is where the capacitors are interconnected together. This node must be connected to the pole V- which is enclosed in the box. This pole can be connected from all sides of the unit capacitor. It simplifies the interconnection and minimizes metal crossings. The second terminal of the cage capacitor V+ is connected using metal 1, because it is a longest distance between metals 1 and 3.

5. Post-layout Simulation Results

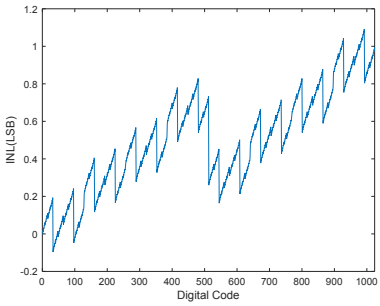
Figures 4a and 4b show a post-layout calculation of the DNL and INL based on definitions [3] of the 10-bit split capacitor DAC layout. Figures 4c and 4d show the same calculation for the 8-bit binary-weighted DAC layout. The parasitics have been extracted using the Cadence Assura tool. Only the post-layout simulation results are provided because CDAC is part of SAR ADC and it is not possible to measure CDAC directly. However, the 10-bit SAR ADC has been already tested and works correctly. A 8-bit SAR ADC fabrication is currently in progress. Differential non-linearity is held below 1/2 LSB and integral non-linearity is around 1 LSB at the maximum magnitude. This is still acceptable for the requirements of the target application. Furthermore, a random mismatch variation of the MIM capacitors has been verified using the Monte Carlo simulation (layout independent) without distortion of the 10-bit CDAC performance. The simulated speed was for 10-bit CDAC at 250 ksps and for 8-bit CDAC at 10 Msps.

6. Conclusion

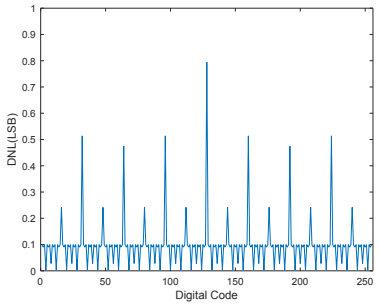
The performance of SAR ADC depends among other factors on the quality of CDAC. To size the unit capacitor proportionally and keep a proper layout style is important to guarantee linearity



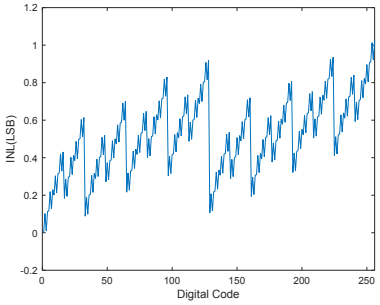
(a) DNL of the 10-bit split CDAC



(b) INL of the 10-bit split CDAC



(c) DNL of the 8-bit binary-weighted CDAC



(d) INL of the 8-bit binary-weighted CDAC

Figure 4: Post-layout simulation results

of the CDAC. No layout style example for a pixel detector application does not exist in the available literature. The 10-bit split CDAC and 8-bit binary- weighted CDAC new layout styles for a pixel detector have been presented. A new MOM capacitor has been proposed. The proposed MOM capacitor, in comparison with [1], provides a better parasitic capacitance shielding and a higher capacitance per area. Simulations have proven that INL and DNL are kept at an acceptable level. Both of the proposed CDAC designs are used in real SAR ADC for radiation imaging detectors.

7. Acknowledgment

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