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A 130 nm CMOS PLL for Phase-II ATLAS-MDT TDC

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The high luminosity and interaction rate expected from the planned High Luminosity-Large Hadron Collider (HL-LHC) upgrade require a replacement and improvement of the ATLAS Muon-Drift-Tube (MDT) read-out electronics. This paper presents a Phase Locked Loop (ePLL) intended to be used inside the improved Time-to-Digital Converter (TDC), which digitizes the arrival time and charge amplitude information. Starting from a 40 MHz input clock, the ePLL provides output clocks of 160 MHz and 320 MHz with a phase resolution of 11.25° and 22.5°, respectively. The prototype, integrated in 130 nm CMOS technology, has 0.02 mm^2 of area and 1.2V of supply voltage.

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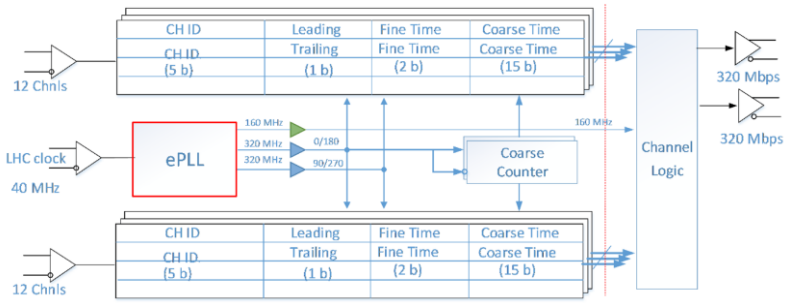

Figure 1. TDC block diagram.

1. Introduction

The high event rate and large amount of data expected from the Phase II Upgrade of High-Luminosity LHC (HL-LHC) imposes challenging requirements for the detectors and the read-out electronics of ATLAS Muon-Drift-Tube (MDT) chambers. Moreover, ATLAS plans to use the MDT detector at the first-trigger level to improve the muon transverse momentum resolution and reduce the trigger rate. The new MDT trigger and readout system will have an output event rate of 1 MHz and a latency of 6 μs at the first-level trigger. Therefore, the read-out electronics must be improved in order to satisfy the new challenging requirements.

The electronic front-end performs amplification, shaping and discrimination through the ASD (Amplification-Shaper-Discriminator) blocks [1]; then the ASD output binary differential signals are provided to a Time-to-Digital Converter (TDC), where the arrival times of leading and trailing edges are digitized in a time bin of 0.78 ns which leads to an RMS timing error of 0.25 ns. The pulse height is encoded as the time interval between the leading and trailing edges of the ASD output pulse.

The Phase Locked Loop (ePLL) presented here will be used for the fine time measurements of the upgraded TDC [3], characterized by a different 130 nm CMOS technology and improved architecture to cope with the Phase II Upgrade requirements. Therefore, the proposed ePLL maintains the same topology of the current one [2] used in the TDC, however with a re-design block by block and optimization, due to the different technology and TDC requirements. A simplified diagram of the new TDC is shown in Figure 1, where the main ePLL task is to provide only two clocks at 320 MHz with adjustable phases; the TDC input signals coming from ASD channels are then used to sample these phase-shifted clocks to determine the hit arrival times. A stand-alone ePLL prototype has been integrated to validate through specific measurements the ePLL operation, in order to include it in the next upgraded TDC version.

The paper is organized as follows. Section 2 describes the ePLL architecture, Section 3 shows some preliminary measurement results, followed by conclusions.

2. ePLL Architecture

The architecture of the presented ePLL is shown in Figure 2. The input clock of 40 MHz is fed to a Phase Frequency Detector (PFD), together with the feedback signal coming from the Phase Shifter block, which acts as a frequency divider with a divider ratio of 8. The up and down signals generated by the PFD have a duration linearly depending from the phase difference

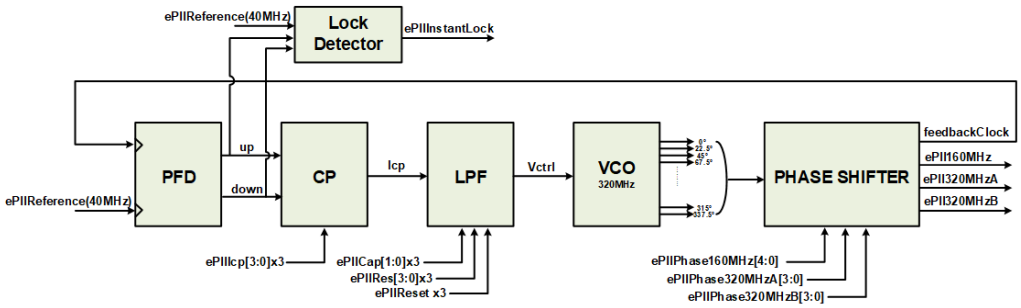

Figure 2. ePLL block diagram.

between the two input clocks. The PFD is composed by two edge detectors and a NOR gate to reset both of them.

The Charge Pump (CP) converts the up and down signals to a current pulse I_{cp}, which is steered through a 1st order Low Pass Filter (LPF) to generate a control voltage V_{ctrl} for the Voltage Controlled Oscillator (VCO). According to the up and down signals, I_{cp} can flow out/into the LPF, discharging/charging the filter capacitor and increasing/decreasing the V_{ctrl} voltage.

The VCO is an 8-stage differential ring oscillator, composed by the cascade of 8 delay cells. The V_{ctrl} signal leads to a variation of the cells delay in order to obtain in lock condition the desired oscillation frequency, i.e. 320MHz. Then, using inverting stages, all the 16 phases of 320 MHz clock are generated, with a phase resolution of 22.5° (i.e. ~195 ps time resolution).

The Phase Shifter block has been optimized and simplified compared to the original one, since in the TDC the only required VCO frequency is 320 MHz with an input (and feedback) frequency of 40MHz. For this reason, a proper Verilog code has been written so that the synthesized Phase Shifter block behaves as a frequency divider with a fixed divider ratio of 8 to generate the 40 MHz feedback clock, reducing complexity and, consequently, power consumption. Then, the Phase Shifter uses the 16 phase-shifted clocks provided by the VCO to generate two 320 MHz output clocks and one 160 MHz clock with programmable phase resolution of 22.5° and 11.25° respectively. The output phases can be selected through 4-bits words for the 320 MHz output clocks, and 5-bits words for the 160 MHz output clock.

Finally, a Lock Detector block controls and indicates when the ePLL lock condition is reached. In order to provide and read the input and output clocks, differential SLVS I/O drivers [4] have been used.

In order to compensate for technology and temperature variations on the loop behavior, the CP output current can be programmed by means of 4-bits word. A 4-bits current-output DAC allows to select the value of the CP output current between 15 possible values, from 8 µA to 120 µA with steps of 8 µA. For the same reason, resistance and capacitance of the LPF can be tuned with 4-bits and 2-bits words respectively. In particular, the resistance is made of 16 resistors and bits-controlled switches and can assume values from 500 Ω to 8 kΩ in steps of 500 Ω; the capacitance can be chosen in a set of 4 values, 30 pF, 40 pF, 50 pF and 70 pF.

3. Measurements

A ePLL prototype has been integrated in 130 nm CMOS technology, in order to validate the circuit performance for future integration in the improved TDC. The layout and floorplan of the integrated ePLL is shown in Figure 3, with a core area of 0.02 mm^2. The power consumption is

Table 1. Performance comparison between the proposed ePLL and the previous one.

	New ePLL	**Previous PLL**
VCO frequency	**320 MHz**	321 MHz
VCO step delay	**195.06 ps**	193 ps
ePLL 160MHz clock frequency	**160.3 MHz**	161 MHz
ePLL 320MHz A,B clock frequency	**320.2 MHz**	321 MHz
Feedback frequency	**39.97 MHz**	40.1 MHz
Lock Control Voltage	**460 mV**	620 mV

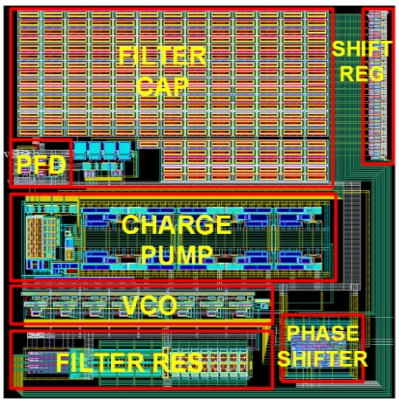

Figure 3. ePLL Layout.

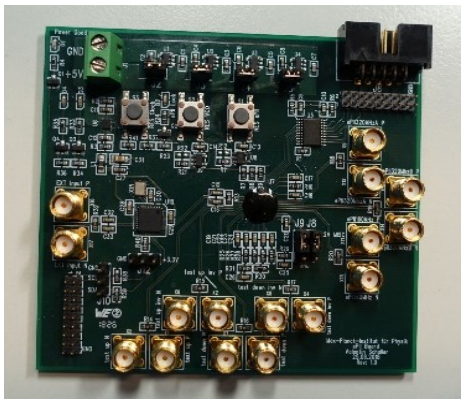

Figure 4. Test board for ePLL measurements.

12.5 mW, for a supply voltage of 1.2 V. A performance comparison with the previous version of the ePLL is reported in Table 1.

Figure 4 reports a photo of the PCB realized for the tests on the ePLL prototype. Measurements show that the three output clocks are always available with programmable phase that can be changed externally, thanks to a serial interface integrated together with the ePLL, to set all the input words.

The measurement of the programmable output phase of the 320 MHz output clock in comparison with the ideal one is shown in Figure 5. The phase steps are almost close to the ideal 22.5°, expect for the range from 180° to 270°. The same can be observed for the 160 MHz output clock, whose measured phases are shown in Figure 6. This non-linearity in the phase shift is confirmed by the DNL, which shows a maximum variation around 0.5% in both cases. The DNL for both the 320 MHz and 160 MHz output clocks are reported in Figure 7 and Figure 8. The non-linearity has been fixed improving the ePLL output stage, i.e. the Phase Shifter; the modified ePLL has been already integrated and submitted.

4. Conclusions

This paper presented a Phase Locked Loop imported and re-designed in order to replace the current ePLL in the upgraded version of the Time-to-Digital Converter for the ATLAS MDT Chambers at HL-LHC. A first ePLL stand-alone prototype has been integrated in 130 nm CMOS technology and a first set of measurements have been performed. The performance results are promising; other complete measurements are carrying on. An improved version of the ePLL,

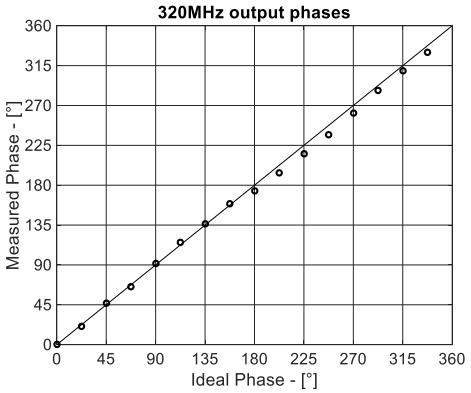

Figure 5. Measured programmable phases for 320MHz output clock.

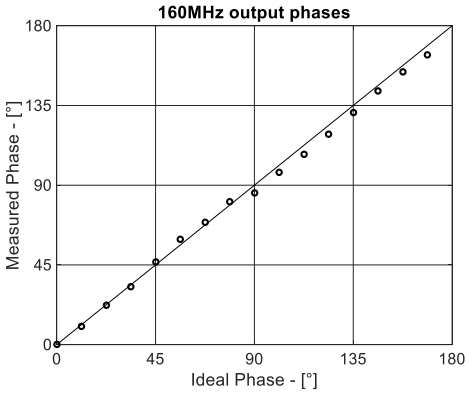

Figure 6. Measured programmable phases for 160MHz output clock.

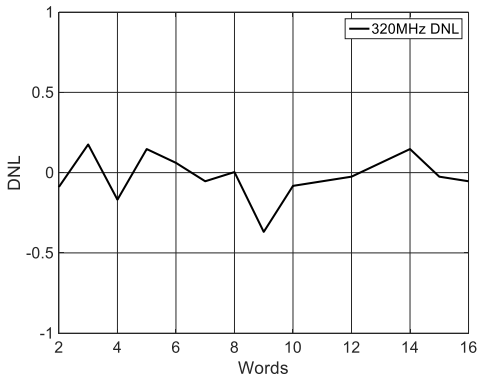

Figure 7. DNL of the measured 320MHz output clocks.

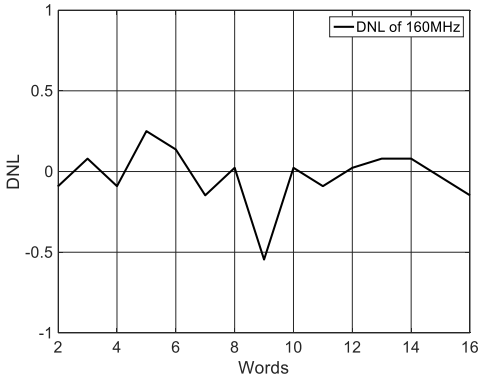

Figure 8. DNL of the measured 160MHz output clocks.

containing some modifications to improve the phase programmability, has been already submitted and is being manufactured.

Aknowledgement

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