PROCEEDINGS OF SCIENCE

Input Mezzanine Board for the Fast Tracker (FTK) at ATLAS

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At LHC Run 2, which started operation in June 2015 at a center-of-mass energy of 13 TeV, the peak luminosity has exceeded $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and the LHC produce an average of 60 simultaneous collisions. The higher luminosity demands a more sophisticated trigger system with increased use of tracking information.
The Fast Tracker (FTK) is an integral part of the trigger upgrade program for the ATLAS experiment. The FTK is a massively parallel hardware system using ASICs and FPGAs. It operates at the full Level-1 accepted rate of up to 100 kHz and provides full event track reconstruction for all tracks with $p_{\mathrm{T}} > 1$ GeV with an average latency below 100 µs. The FTK Input Mezzanine Board is the input interface of the FTK system which performs full reconstruction of all clusters in the ATLAS Inner Detector. These proceedings report details of the functionality of the FTK Input Mezzanine Board and its status of installation and commissioning.

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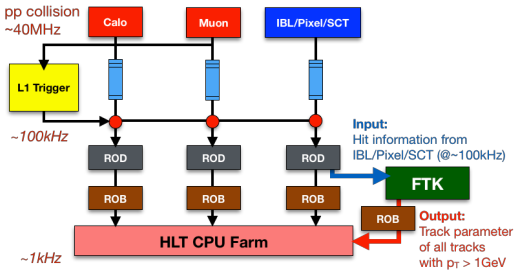
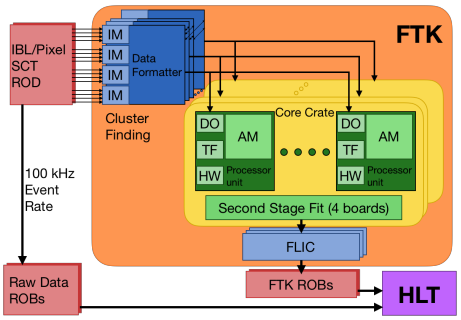
1. Introduction

In the Large Hadron Collider (LHC) experiments, it is important to control trigger rate while keeping interesting physics events. ATLAS [1] uses a two-level trigger system. The Level-1 (L1) trigger is a hardware based trigger, which consists of hits in muon spectrometer and energy deposition in electromagnetic and hadronic calorimeter. It reduces trigger rate to around 100 kHz. After L1 decision, CPU-based High Level Trigger (HLT) further reduces trigger rate to around 1 kHz. So far, the ATLAS trigger system has worked well and it has brought a lot of fruitful results such as the recent observation of $H \to b\bar{b}$ and $t\bar{t}H$ [2, 3]. To improve physics sensitivity, the luminosity of the LHC will become higher. It can accumulate more data, although it will cause multiple proton-proton interactions per bunch crossing, so called pile-up. As a result of the pile-up, signal and background separation becomes harder. Fine resolution tracking information is essential to identify signal and pile-up vertices. However, full event track reconstruction is prohibitively expensive in terms of processing resources.

The Fast Tracker (FTK) [4] is a newly installed hardware based tracking system with massive parallel processing. Figure 1a shows an overview of the ATLAS trigger system with the FTK, which is installed between L1 and HLT. The FTK receives all hit information from the insertable b-layer (IBL [5]), the Pixel and the SemiConductor Tracker (SCT) [1] with L1 accepted rate of up to 100 kHz, and provides all track information with $p_{\mathrm{T}} > 1$ GeV at the beginning of HLT processing within $\sim 100\,\mu$s. A functional sketch of the FTK system is shown in Figure 1b. These proceedings focus on the FTK Input Mezzanine Board (IM) which is the input interface and the first processing stage of the FTK system.



(a)



(b)

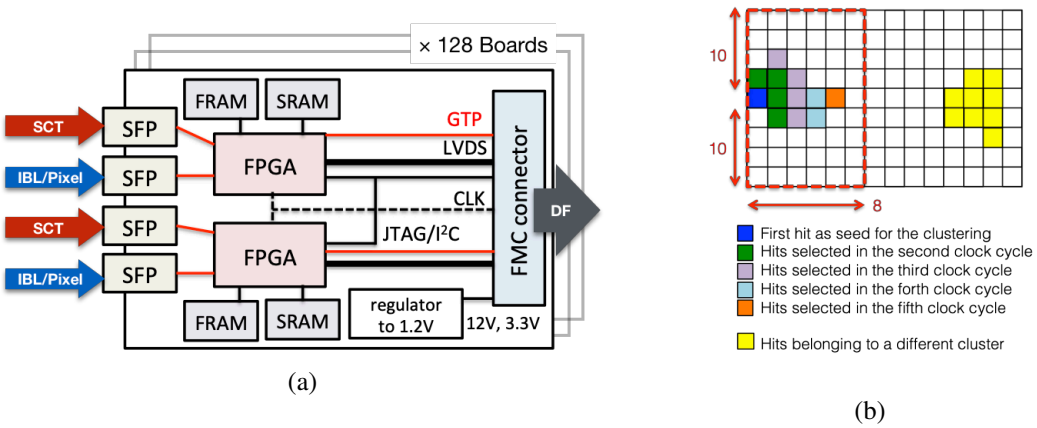
Figure 1: (a) An overview of the ATLAS trigger system. ROD is the read-out driver and ROB is the read-out buffer. The FTK system (green) is installed between L1 and HLT. (b) A functional sketch of the FTK system [4]. AM is the Associative Memory, DO is the Data Organizer, TF is the Track Fitter, HW is the Hit Warrior, and FLIC is the FTK-to-Level-2 Interface Crate. Each function is described in more detail in [4]. The FTK Input Mezzanine (IM) is the input interface and the first processing stage of the FTK system, which is mounted on the Data Formatter (DF) motherboard.

2. Functionality of the FTK Input Mezzanine Board

The main functions of the IM are: to receive the IBL, Pixel and SCT data from the ATLAS silicon read-out drivers (RODs) with around 100 million channels, to perform clustering to reduce

data size, and to forward the data to the Data Formatter (DF) motherboard. In total 128 IMs are required to manage all data from the RODs. Figure 2a shows an overview of the components and the lines of the IM. The IM functions are implemented in a mezzanine card of 12 layers with a size of 149 mm $\times$ 74 mm which connects the DF with a High Pin Count FPGA Mezzanine Card (FMC) connector. The IM receives the ROD data with the rate of up to 4×2.0 Gbps by four SLINK optical fibers through four SFP+ connectors. To implement the IM functionality, two FPGAs are mounted on each IM. Each FPGA handles two input lines; one from the IBL/Pixel, and another from the SCT ROD. Each line processes the data independently. Each FPGA is equipped with a 18 Mb external SRAM and a 32 Mb flash memory. Each FPGA is connected with the DF by four fast GTP lines, which is Xilinx high-speed serial transceiver with the rate up to 3.1 Gbps, and 16 LVDS lines. For transmitting the output to the DF, the FPGA uses LVDS lines with 200 MHz Double Data Rate (DDR). The IM slow control and monitoring system are built by the Inter Integrated Circuit (I2C) bus from the DF. Power with local regulator and JTAG lines are connected via a FMC connector.

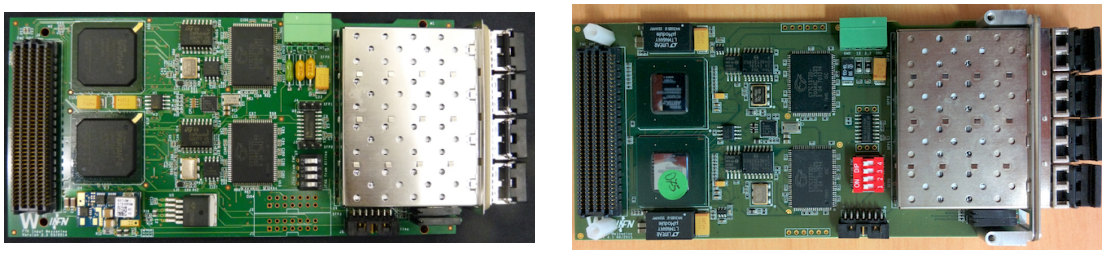
In the FPGA, a custom clustering algorithm [6] is implemented. Figure 2b shows an overview of the clustering algorithm. The cluster finding logic starts with the first received hit. It defines a window (21×8 pixel size) with respect to the first hit position. Then the logic loads all hits within the window. Once all the hit data are loaded, the algorithm selects the first reference hit. Then on each clock cycle, the hits in direct neighborhood with the selected hit are selected until no directly neighboring hits remain. Eventually all selected hits are clustered and its size and centroid information are passed to DF. It reduces the size of input data by around 60 % keeping hit position information.



(a) (b)

Figure 2: (a) An overview of the components and the lines of the IM. (b) An overview of the pixel clustering algorithm.

Figure 3 shows the photographs of the IM. Because the IBL hit occupancy is higher than Pixel, two types of the IM implementation are prepared. The two designs are the same except their FPGAs. The left one has Spartan-6 (XC6SLX150T) and the right one has Artix-7 (XC7A200T) FPGA. Because Artix-7 has more FPGA resources than Spartan-6, the IM with Artix-7 can be used for both the IBL and Pixel hit processing and the one with Spartan-6 can be used for the Pixel hit processing.



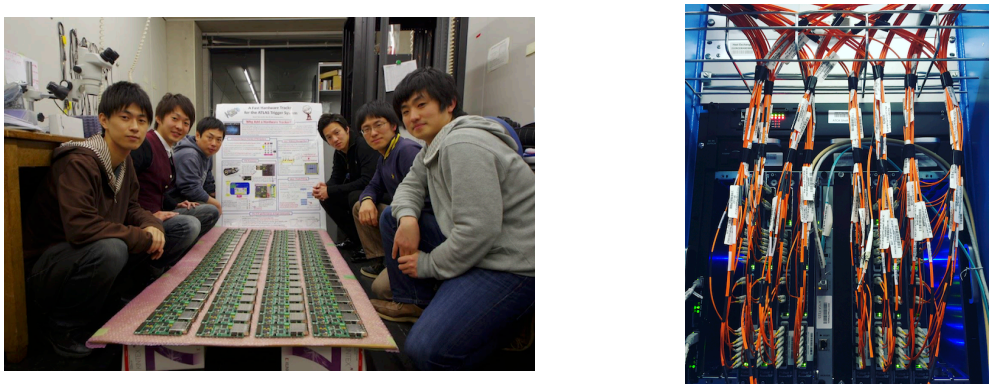
(a) (b)

Figure 3: Photographs of IM. (a) Two Spartan-6 (XC6SLX150T) FPGAs are implemented. (b) Two Artix-7 (XC7A200T) FPGAs are implemented.

3. Status of Installation and Commissioning

The IM mass production and quality control tests are completed. The contents of the tests are visual checks, electrical checks, and bit-error-rate (BER) measurements. All produced IMs passed the tests satisfying the ATLAS requirements of BER of 10^{-15}. Figure 4a shows the photograph after mass production of the IMs with Spartan-6.

Commissioning of the FTK system started from 2015. All IMs are mounted on DFs and they are installed in the ATLAS DAQ. The cabling with the IBL, Pixel and SCT ROD are completed. Figure 4b shows the photograph of IMs and DFs in the ATLAS DAQ. Real data taking of IM with the IBL, Pixel and SCT was established with input rate up to 100 kHz. Online configuration and monitoring tools for IM are implemented and used for commissioning. Dataflow tests with a slice of the FTK system are ongoing. In August 2018, it was succeeded to build dataflow throughout a slice of the FTK system and to send the 12-layer track information to the ATLAS Readout System. The next goal is to establish the dataflow stability of the entire system with high parallelization.



(a) (b)

Figure 4: (a) Photograph after mass production of the IMs. (b) All IM and DF boards are installed in the ATLAS DAQ.

4. Further Improvements of the FTK Input Mezzanine Board

Main functions in the IM firmware was established after extensive dataflow tests with real

data. To utilize the FPGA resources efficiently, the IM firmware code was refactored keeping its functionality. Unnecessary functions were removed, which were only used for debugging during the firmware development, and the clock signals were carefully treated. All firmware code were reviewed by engineers from SLAC. Firmware refactoring improves readability and timing constraints and saves around 20 % FPGA resources.

The remaining challenge is improvements of the clustering algorithm. Very occasionally, there are long sequential hits on both IBL and Pixel, which is due to beam-halo and delta ray. It takes long time to perform clustering for these hits. Therefore such hits should be removed before clustering. To achieve this goal, buffers are defined in the firmware which count the number of hits in each column and row of IBL and Pixel. If the number of hits in a column or a row exceeds a defined threshold, all hits in the column or row are removed. The processing time is reduced by this method and its effects to tracking performance are under investigation. In addition, the Time over Threshold information (ToT) in IBL and Pixel could be used for the clustering algorithm. Because ToT depends on particle energy deposition, it could distinguish the particle hit position from electronics noise and improve the accuracy of the hit position.

5. Conclusion

In these proceedings the functionality and current development status of the IM are described. The IM is the input interface of the entire FTK system. The IM mass production and installation were completed. Dataflow tests with the entire FTK system are ongoing. Further improvements of the IM are discussed. Dataflow with 25% of the entire system will be established in 2018 and will be upgraded during LHC shutdown from 2019 to 2020.

References

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