

# ATLAS Phase-II-Upgrade Pixel Demonstrator Read-out

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The ATLAS tracking system will be replaced by the all-silicon inner-tracker (ITk) consisting of pixels and strips in the course of the HL-LHC upgrade until 2026. The readout of the ITk pixel system will be most challenging in terms of data rate. First test of readout concepts are performed with the *ITk Pixel Demonstrator*, a system composed of several ITk-style modules with 120 readout chips in total. Their readout is realised with data aggregation via GBTx chips transmitting data optically to ATCA-boards acting as off-detector components.

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## 1. Introduction

The upgrade of the ATLAS detector with the all-silicon inner-tracker (ITk) [1] will increase the per-link data rates from currently up to 160 Mbit/s to up to 5.12 Gbit/s. The Outer Barrel Demonstrator gives the opportunity to test readout systems with similar bandwidths by aggregating data from several modules.

## 2. Outer Barrel Demonstrator

The Outer Barrel Demonstrator is an effort to build a stave similar to the staves in the outer barrel region of the ITk to gain knowledge on how to build and operate such a system.

This version of the demonstrator is equipped with 120 FE-I4B chips [2], which is the frontend chip currently used in the ATLAS pixel detector in the insertable B-layer [3] and operates at 160 Mbit/s. The frontends are arranged in double or quad-chip modules and the modules are powered serially.

The demonstrator will also serve as testbed for readout development and by aggregating multiple frontend channels, multi-gigabit data rates similar to those of ITk modules can be achieved (3.2 Gbit/s for 20 FE-I4B compared to 1.28-5.12 Gbit/s for one ITk pixel frontend chip). First tests were performed on a smaller stave with 7 quad-chip modules while the full demonstrator is still under construction.

The final readout chip for the ITk pixel upgrade will be based on the RD53A prototype chip and a demonstrator with the RD53A and a different readout and aggregation scheme will be built in the future.

## 3. Demonstrator Readout

### 3.1 RCE-GBT Readout System

Several readout systems are used for the demonstrator. This description will focus on the RCE-GBT readout system.

The GBTx is a radiation hard chip for HEP applications which implements a bidirectional optical link [4]. It aggregates several low bandwidth electrical links (e-links) with up to 320 Mbit/s into one fast optical link with 3.2 Gbit/s user bandwidth. It also provides some forward error correction on the optical link.

The RCE (Reconfigurable Cluster Element) platform is a readout system which uses processing units (RCEs) with the Xilinx Zynq system on chip. RCE-GBT is a variant of the RCE system which interfaces to GBTx chips via optical links to read out the aggregated channels.

The RCE COB (Cluster on Board) is an ATCA based version of the RCE readout system. It houses up to four Data Processing Modules (DPM), which provide two RCEs each. The readout and data analysis is performed directly on the RCEs, while the system is controlled via the network. Each DPM has two optical links, one to each RCE. A COB with 3 DPMs is sufficient to read out the full demonstrator.

### 3.2 Readout Architecture

The 60 frontends on each side of the demonstrator are organized in 16 double and 7 quad-chip modules, with the same layout and connectivity on both sides. Connection to the demonstrator is provided via VHDCI connectors with 12 or 16 channels each, corresponding to four quads (16 channels), three quads (12 channels), or 8 doubles (16 channels). The pinout of the connector was chosen such that double and quad connectors are interchangeable on the readout side. Those connectors are the common interface to the demonstrator for all readout systems and adapters on the readout side have to accommodate for this.

Each module is connected via differential clock and command lines from the readout, as well as 2 data pairs for a double-chip and 4 data pairs to the readout for a quad-chip module. As the modules are operated in a serial powering setup, AC coupling of all signals is mandatory.

At 160 Mbit/s per channel, the GBTx can support 20 channels which means that at least 6 GBTx are required to read out the full demonstrator. And due to the different number of channels per connector, additional mapping is required to get the minimal number of GBTx. This is achieved by splitting the 20 channels into 16 and 4, where the 16 channels are connected directly to the VHDCI, and the 4 remaining channels are combined across 3 GBTx with a passive adapter to provide the 12 channel connector.

The GBTx are then connected optically to the readout. The overall readout scheme is shown in Figure 1.

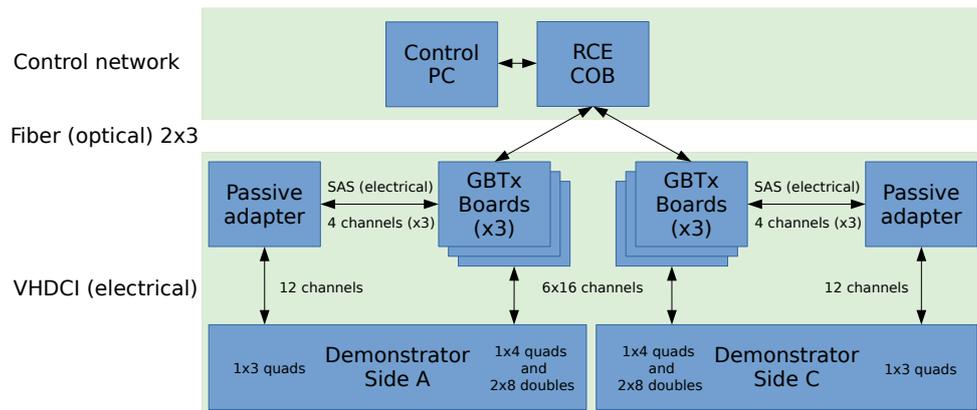


Figure 1: Readout architecture for the demonstrator with RCE-GBT.

### 3.3 Adapter Boards

The first version of the adapter boards was based on the Versatile Link Demonstrator Board, an evaluation board for the GBTx [4]. This board provides the channels on HDMI-connectors, which required additional adapters, made the setup very large and unwieldy, and caused significant signal degradation. Therefore, a new version which avoids those issues was developed.

The current approach is based on GBT mezzanine boards originally developed as end-of-substructure card prototype for ITk strips. By using an existing and already working design, the prototyping is simplified and the development effort is greatly reduced.

The mezzanine board is wire-bonded to a custom carrier board which provides the electrical connection via VHDCI and performs AC coupling. The optical link is implemented via an SFP-transceiver directly plugged into the mezzanine. This is shown in Figure 2. The additional channels of the GBTx are broken out on a mini-SAS connector and can be bundled with other GBTx.



Figure 2: Carrier board with mezzanine, VHDCI cable to the demonstrator on the left, and optical link to the readout on the right.

### 3.4 Short Electrical Prototype

The short electrical prototype is a smaller stave with 7 quad modules in a serial powering chain and is used as test setup before the construction of the full demonstrator is finished. The stave is shown in Figure 3.



Figure 3: Short electrical prototype with 7 quad modules.

## 4. Test Results

A range of tests and scans were performed on the short electrical prototype to verify that the modules can be operated properly using the RCE system and to test the operation of the GBTx adapter boards. Two of the frontends are known to be non-functional from prior tests.

The basis for most scans are the digital and analog tests, where a signal is injected internally into the digital or analog part of each frontend pixel and allows to test the response of every pixel. This also serves as a basic test of the link to the frontend. An example of an analog test is shown in Figure 4a, where most of the pixels show the expected number of injections. Additionally, the

modules were tuned to a specific pixel discriminator threshold and time over threshold response. The thresholds are shown in Figure 4b. Most of the frontends are tuned properly to a threshold of 3000 e. Up to 24 out of the 28 frontends on the 7 modules were read out in parallel using two GBTx-boards, which can also be seen in Figure 4b. The other four frontends were broken or had to be disabled for stable operation. A test with a radioactive  $^{90}\text{Sr}$  source was also performed, which is shown in Figure 4c. Some mechanical features, components and traces on the flex on top of the module are visible.

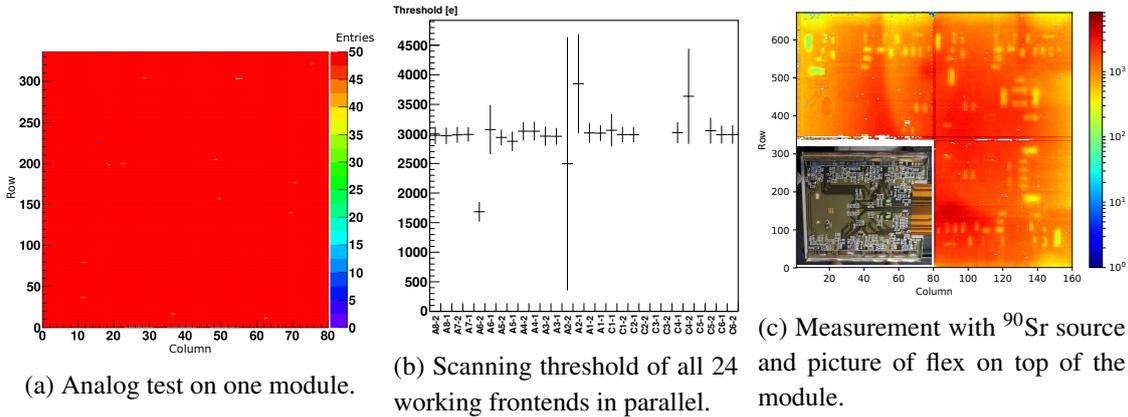


Figure 4: Results from tests.

## 5. Conclusion and Outlook

The tests with the short prototype have shown that the proposed readout scheme is a viable option for the full demonstrator and scaling up the system can be achieved by adding more GBTx boards. No major issues with the GBTx boards were discovered and the final version of the board will include only a few small improvements. Overall, the new boards are a big improvement over the previous approach with the VLDB and can provide compact and modular readout for the demonstrator.

The setup for the full demonstrator will also be mounted in a rack and equipped with additional hardware to allow remote configuration of the GBTx and dedicated power supplies. Further tests are also needed to test the system under high bandwidth conditions and to check the signal integrity of the full system.

## References

- [1] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, CERN-LHCC-2017-021; ATLAS-TDR-030
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