PROCEEDINGS OF SCIENCE

# CMS ECAL Upgrade Front End card: design and prototype test results

**A.Dolgopolov**
*Fermilab*
*USA*
*E-mail:* alexandre.dolgopolov@cern.ch
**C.Jessop**
*University of Notre Dame*
*USA*
*E-mail:* colin.jessop@cern.ch
**N.Loukas**
*University of Notre Dame*
*USA*
*E-mail:* nikitas.loukas@cern.ch
**A.Singovski**[1]
*University of Minnesota & University of Notre Dame*
*USA*
*E-mail:* alexander.singovski@cern.ch

*On behalf of the CMS Collaboration*

The CMS ECAL Phase 2 Front-End (FE) card is designed to provide streaming of digitized data generated on the Very-Frond-End (VFE) cards to the CMS ECAL back-end electronics system based on the Barrel Calorimeter Processor (BCP) ATCA modules. The FE card is intended to utilize data links developed within the Versatile Link common project. The card will contain four lpGBT ASICS with corresponding versatile link plus optical link modules.
The first prototype FE card was developed to validate the clock distribution, the high speed serial data links as well as other specific technical features of the future design using the currently available GBT chipset and versatile link components.

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[1]Speaker





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## 1. Introduction

The High Luminosity project at CERN (HL-LHC)[1] will deliver an unprecedent amount of data to the detectors. The instantaneous luminosity will be more than 5 times higher than the LHC design, up to 7.5 x $10^{34}$cm$^{-2}$s$^{-1}$, while the luminosity integrated over 3 runs of HL-LHC data taking will be 10 times higher than that expected for the Phase 1 LHC program, 3000fb$^{-1}$.

This imposes a challenging requirements for the LHC detectors. In particular the readout electronics. The detector performance should be at least maintained at the same level as the LHC run1 performance. It also can be improved in some aspects to provide required data quality in the much harder radiation load and pileup conditions. In the case of the CMS [2] barrel calorimeter this will be achieved by better signal handling without replacement of the detector elements.

## 2. Upgrade VFE requirements

The key features of the upgrade of the on-detector electronics are the fast Trans-Impedance Amplifier with the picking time of 20ns, 12 bit ADC running at 160MHz sampling rate, and dead-time-less data streaming off-detector for triggering and recording. The fast readout will allow on-line detection of the anomalous APD signals (spikes) and will provide 30ps time resolution required for pileup mitigation.

### 2.1 Data rates

The legacy Very-Front-End (VFE)[2] electronics generate 14 bits information per calorimeter channel (crystal) at 40MHz rate: a 12 bit ADC plus 2 bits for preamplifier gain of 1, 6 or 12. This results in 14Gb/s data rate for each Front-End (FE)[2] card, serving to stream the data from one Trigger Tower (5x5 crystals). As the data transmission cannot support this rate, we have to apply a Level1 trigger for data flow reduction. The upgrade VFE card will run at 160MHz sampling to cope with the high pileup and provide better time resolution. It will generate 13 bits data per clock: 12 bits ADC plus 1 bit for preamplifier gain of 1 or 10. The ECAL barrel detector elements, crystals and APDs, allow this improvement, as demonstrated by realistic tests, including ones with a beam. Hence, the target FE data transmission rate is 13bits@160Mhs x 25 channels per tower – 52Gb/s. To cope with such a rate we should first use the next generation radiation tolerant data encoders, lpGBT[3], running at 10Gb/s, and second apply some data reduction / compression procedure at VFE level. The legacy and upgrade VFE electronics designs and the corresponding data rates are summarized in figure1 and table1.

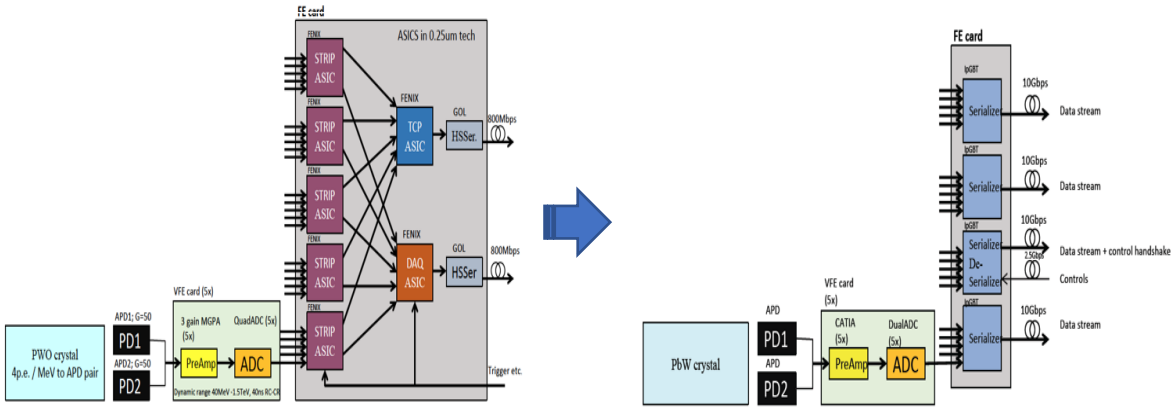


*Figure 1. Schematic view of the ECAL barrel on-detector electronics upgrade.*

| | Legacy on-detector electronics | Upgrade on-detector electronics |
|---|---|---|
| Sampling rate | 40 MHz | 160 MHz |
| Bits per channel | 14 | 13 |
| Data rate per crystal | 560 Mb/s | 2080 Mb/s |
| Data rate per FE card: 25 crystals | 14 Gb/s | 52 Gb/s |
| Data readout rate | With Level1 trigger:<br>Data – 0.8Gb/s<br>Trigger primitives – 0.8 Mb/s | With compression:<br>Data – 32Gb/s |

*Table1. Summary of the data rates for the legacy and upgrade VFE electronics.*

### 2.2 Up-links

The lpGBT serializer is designed to send a 256 bits frame at 40 MHz rate. 224 bits of the frame can be used for the user data. The data from one calorimeter cell, 13bits@160MHz, will be compressed by the Data Transmission Unit (DTU) from 52 bits@40MHz to 32 bits@40MHz and transmitted to the lpGBT via serial e-link at 1280Mb/s rate, one link per channel. The total amount of data from 25 crystals of one readout tower, served by FE card at 40MHz will be 32x25=800 bits. This data fits into four lpGBT frames. The schematics of the ADC-to-off detector data transmission is presented in figure 2.

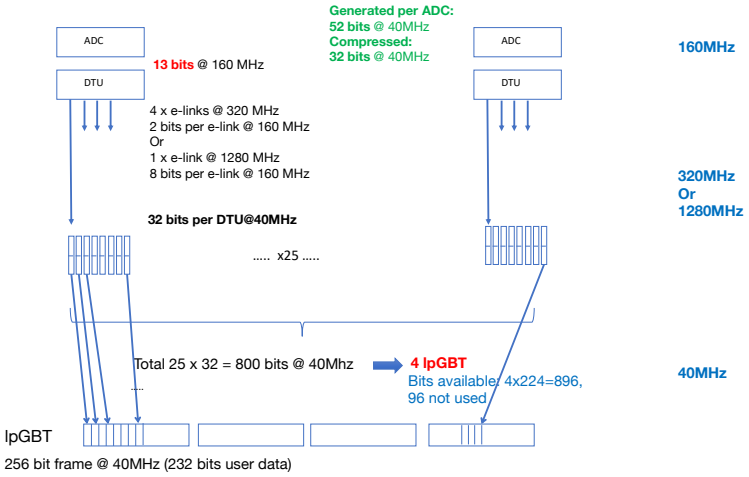


*Figure 2. Schematics of the data flow from ADC to lpGBT serializer.*

One lpGBT chip will work in transceiver mode (Master lpGBT), while three others in transmitter only mode (Slave lpGBT). The serial outputs of all lpGBT chips will be connected to the Versatile Link Plus[4] transceiver module with for transmitters and one receiver channels.

### 2.3 Down links: clock distribution and control functions

The FE card provides initialization and control of all VFE components, precise clock distribution and monitoring of the VFE components. These functions will be implemented via optical down-link and slow control capability of the master lpGBT chip.

The clock to VFE components should be delivered with jitter less than 10 ps, required by the design time resolution of 30ps of the whole detector. Such a high precision requires minimal phase adjustment in the clock path. The clock to all 25 VFE channels will be

distributed from the master lpGBT as down e-link clocks. The other outputs of the same clock will be served as the system clock to slave lpGBT. According to lpGBT design specification, this scheme should provide sufficient clock quality for the stable optical links operation at 10Gb/s rate and required time resolution.

The slow control will be implemented via lpGBT $I^2C$ function. As the number of $I^2C$ masters per chip is not sufficient to serve all required lines, the $I^2C$ bus will be chained over all slave chips. The schematics of the FE clock and control connections is shown in fugure 3.

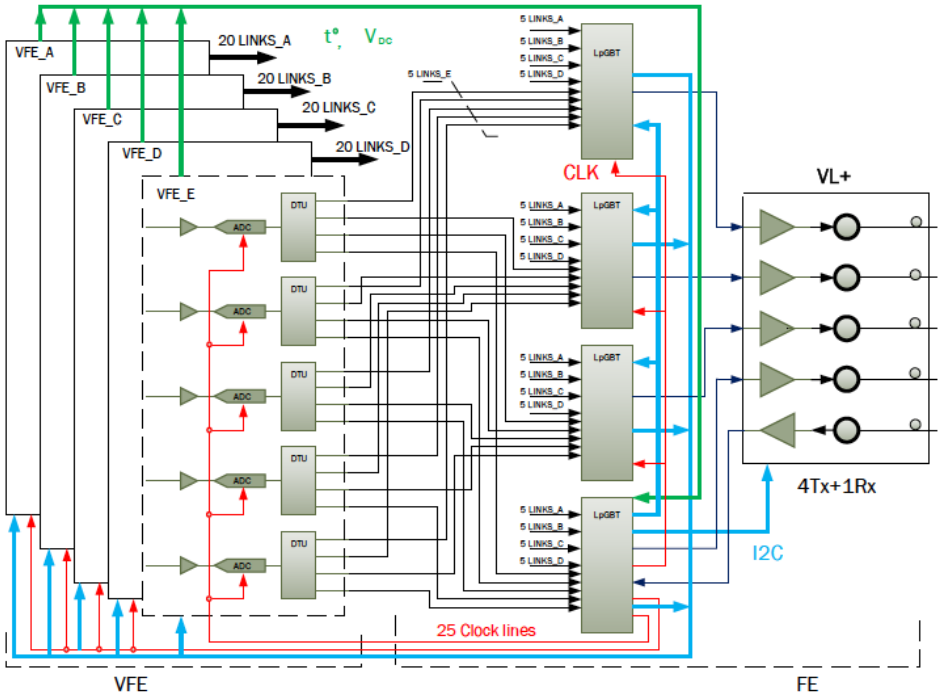


*Figure 3. The clock distribution (red) to the slave lpGBT and VFE components from the master lpGBT e-link clocks. I2C buses (blue): one to Versatile Link Plus transceiver, one to each VFE card, one to Slave lpGBT. Power voltage and temperature control (green) from VFE cards.*

## 4. Upgrade VFE prototype

The key components of the upgrade FE card, lpGBT transceivers and Versatile Link Plus opto-hybrids are not yet available for users. We have designed and produced a FE prototype based on the currently available GBTx transceivers and Versatile Link (VL) hybrids. The card contains five GBTx chips, one GBT-SCA chip and three VL hybrids, one TRx and two TTx.

The maximum up-link data rate of this card is 5 x 3.2Gb/s = 16 Gb/s, sufficient for the legacy VFE data streaming and not sufficient for the upgrade VFE with 160MHz sampling. This prototype allows validation of some aspects of the FE card design where the GBTx features are similar to lpGBT ones: e-link clocks distribution, slow control via optical down-link and voltage and temperature monitoring. The prototype was tested in the laboratory, connected to the ECAL legacy Trigger Tower VFE cards from one side and to the CTP7[5] off-detector card on the other.

### 4.1 Prototype test results

The up-link performance with the system clock delivered to the slave GBTx in the transmitter-only mode via optical down-link and master GBTx in the transceiver mode was tested with all five GBTx in the test configuration. The test patterns were received and decoded by CTP7. The eye diagrams for the master and one slave GBTx are shown in figure 4. The eye opening confirm the stable links operation. Bit Error rate measured by LeCroy SDA820Zi is ~$10^{-13}$

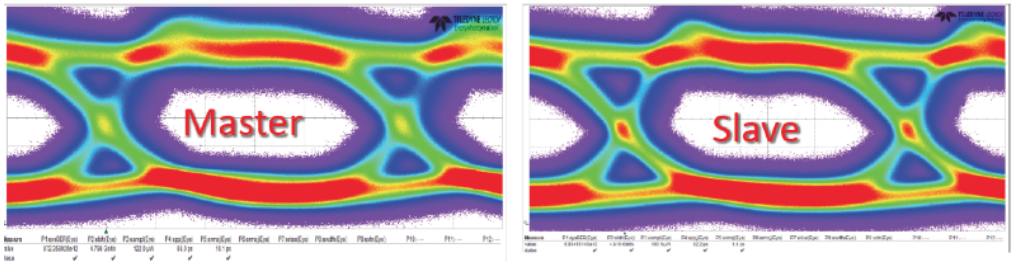


*Figure 4. Eye diagramms of the fast up-link for master GBTx, running in the transciever mode and the slave GBTx, rinning in the transmiter-only mode.*

The jitter measurements of the clock to VFE card, taken from the e-link clock outputs of the master GBTx are shown in figure 5. Clock jitter was calculated by the jitter analysis package of the LeCroy serial data analyzer SDA820Zi. The clock signal was taken from the test points on the FE prototype (point 1) and on the VFE prototype (point 2). The measured jitter is at the 10ps level, well inside specifications

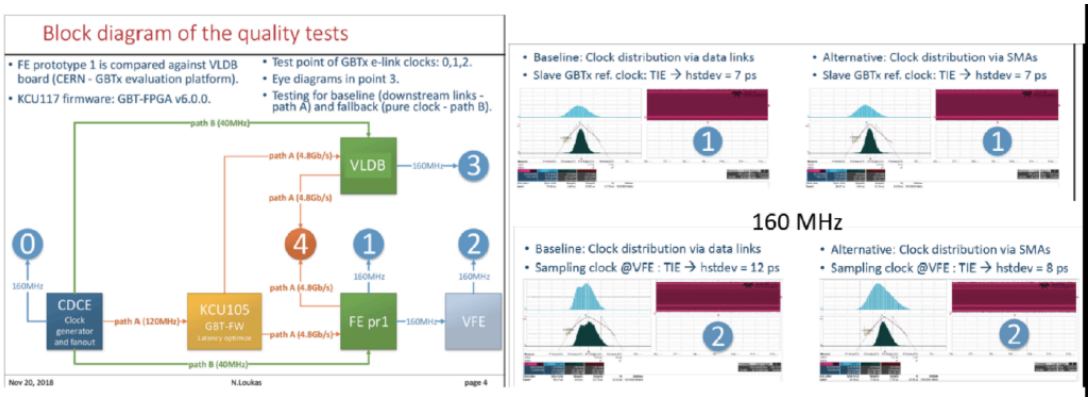


*Figure 5. Schematics of the clock jitter test (left), and the test results: clock jitter on the FE board (right top) and clock jitter on the VFE board (right bottom)*

## References

[1] High-Luminosity Large Hadron Collider (HL-LHC) Technical design report. CERN-2017-007-M

[2] CMS ECAL Technical Design Report (CERN/LHCC 97-33 CMS TDR 4 15 December 1997)

[3] P.Moreira, lpGBT Specifications. https://espace.cern.ch/GBT-Project/LpGBT/Specifications/LpGbtxSpecifications.pdf

[4] C. Soós et al. Versatile Link Plus Transceiver development. Journal of Instrumentation, Volume 12, March 2017, C03068

[5] **A**.Svetec et al. The Calorimeter Trigger Processor Card: the next generation of high speed algorithmic data processing at CMS, Journal of Instrumentation, Volume 11, February 2016, C02011

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